Dual 16-Bit, 1.0 GSPS D/A Converter

Preliminary Technical Data

AD9779

FEATURES

- DAC Output Sample Rate 1GSPS+
- 1.8/3.3 V Single Supply Operation
- Low power: 980mW @ 1GSPS, 600mW @ 500MSPS
- SFDR =82 dBc to f_{OUT} = 100 MHz
- Single Carrier WCDMA ACLR = 79 dBc @ 80 MHz IF
- CMOS data interface with Autotracking Input Timing
- Analog Output: Adjustable 10-30mA (RL=25 Ω to 50 Ω)
- 2×, 4×, 8× Interpolation
- On Chip Coarse Complex Modulator allows $f_{DAC}/2$, $f_{DAC}/4$, $f_{DAC}/8$ Modulation
- Auxiliary DACs allow control of external VGA, Offset Control
- 100-lead Exposed Paddle TQFP Package
- Multiple Chip Synchronization Interface
- 84dB Digital Interpolation Filter Stopband Attenuation
- Digital Inverse Sinc Filter

APPLICATIONS

- Wireless Infrastructure
  - Digital High or Low IF Synthesis
  - Internal Digital Upconversion Capability
  - Transmit Diversity
- Wideband Communications Systems:
  - Point-to-Point Wireless, LMDS
  - Multi Carrier WCDMA
  - Multi Carrier GSM

PRODUCT DESCRIPTION

The AD9779 is a dual 16-bit high dynamic range DAC that provides a sample rate of 1 GSPS, permitting multi carrier generation up to its Nyquist frequency. It includes features optimized for direct conversion transmit applications, including complex digital modulation and gain and offset compensation. The DAC outputs are optimized to interface seamlessly with analog quadrature modulators such as the AD8349. A serial peripheral interface (SPI) provides for programming /readback of many internal parameters. The output current can be programmed over a range of 10mA to 30mA. The AD9779 is manufactured on an advanced 0.18µm CMOS process and operates from 1.8V and 3.3V supplies for a total power consumption of 950mW. It is supplied in a 100-lead TQFP package.

PRODUCT HIGHLIGHTS

Ultra-low noise and Intermodulation Distortion (IMD) enable high quality synthesis of wideband signals from baseband to high intermediate frequencies.

Single-ended CMOS interface supports a maximum input rate of 300 MSPS with 1x interpolation.

Uses a proprietary DAC output switching technique that enhances dynamic performance.

The current outputs of the AD9779 can be easily configured for various single-ended or differential circuit topologies.

FUNCTIONAL BLOCK DIAGRAM

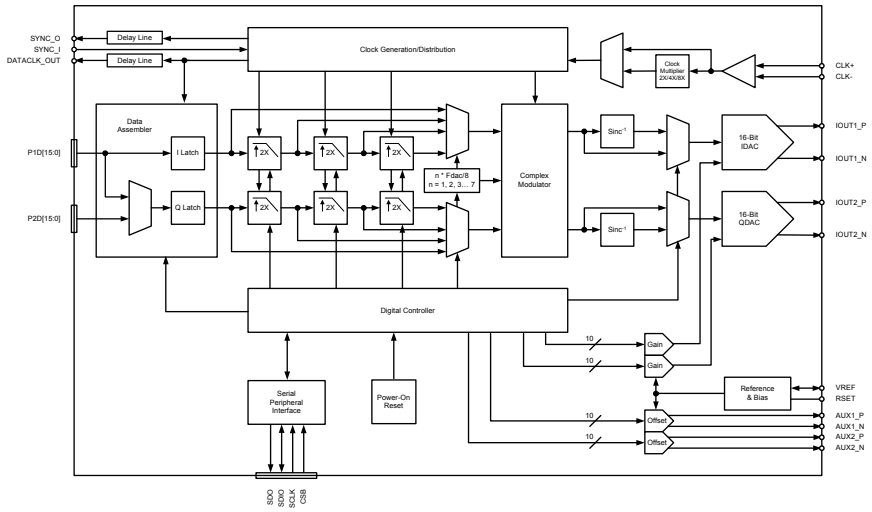

Figure 1 Functional Block Diagram

Rev. PrG

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TABLE OF CONTENTS

REVISION HISTORY

Revision PrA: Initial Version

Revision PrB: Updated Page 1 Features, added eval board schematics, SPI register map, filter coefficients and filter response curves

Revision PrC: Added characterization data, description of modulation modes, internal clock distribution architecture, timing information

Revision PrE: Added more ac characterization data, power dissipation, synchronization, updated evaluation board schematics and PCB

Revision PrF: Added eval board rev D schematics and PCB

Revision PrG: Added lead free and reel designations to ordering guide, fixed error in SPI table, added ESD information, fixed compliance range error, added reset pin description

SPECIFICATIONS[1]

DC SPECIFICATIONS

(VDD33 = 3.3 V, VDD18 = 1.8 V, MAXIMUM SAMPLE RATE, UNLESS OTHERWISE NOTED)

Parameter		Temp	Test Level	Min	Typ	Max	Unit
RESOLUTION					16		Bits
ACCURACY	Differential Nonlinearity (DNL)				± 1.5		LSB
	Integral Nonlinearity (INL)				± 5		LSB
ANALOG OUTPUTS	Offset Error				± TBD		% FSR
	Gain Error (With Internal Reference)				± TBD		% FSR
	Gain Error (Without Internal Reference)				± TBD		% FSR
	Full Scale Output Current			10	20	30	mA
	Output Compliance Range			-1.0		+1.25	V
	Output Resistance				TBD		kΩ
	Output Capacitance				TBD		pF
TEMPERATURE DRIFT	Offset				TBD		ppm/°C
	Gain				TBD		ppm/°C
	Reference Voltage				TBD		ppm/°C
REFERENCE	Internal Reference Voltage				1.2		V
	Output Current				100		nA
ANALOG SUPPLY VOLTAGES	VDDA33			3.13	3.3	3.47	V
DIGITAL SUPPLY VOLTAGES	VDDD33			3.13	3.3	3.47	V
	VDDD18			1.70	1.8	1.90	V
	VDDCLK			1.70	1.8	1.90	V
POWER CONSUMPTION	1.0 GSPS				980		mW
	500 MSPS				600		mW
	Standby Power				TBD		mW

Table 1: DC Specifications

[1] Specifications subject to change without notice

DIGITAL SPECIFICATIONS

(VDD33 = 3.3 V, VDD18 = 1.8 V, MAXIMUM SAMPLE RATE, UNLESS OTHERWISE NOTED)

Parameter		Temp	Test Level	Min	Typ	Max	Unit
DAC CLOCK INPUT (CLK+, CLK-)	Differential peak-to-peak Voltage				800		mV
	Common Mode Voltage				400		mV
	Maximum Clock Rate				1		GSPS
SERIAL PERIPHERAL INTERFACE	Maximum Clock Rate (SCLK)					40	MHz
	Minimum Pulse width high					12.5	ns
	Minimum pulse width low					12.5	ns
INPUT DATA	Set up Time, Input data to DATACLK (all modes)			3.2			ns
	Hold Time, Input data to DATACLK (all modes)			-1.6			ns
	Reference Clock to DATACLK out				5ns		

Table 2: Digital Specifications

AC SPECIFICATIONS

(VDD33 = 3.3 V, VDD18 = 1.8 V, MAXIMUM SAMPLE RATE, UNLESS OTHERWISE NOTED)

Parameter		Temp	Test Level	Min	Typ	Max	Unit
SPURIOUS FREE DYNAMIC RANGE (SFDR)	f_{DAC} = 100 MSPS, f_{OUT} = 20 MHz				82		dBc
	f_{DAC} = 200 MSPS, f_{OUT} = 50 MHz				82		dBc
	f_{DAC} = 400 MSPS, f_{OUT} = 70 MHz				84		dBc
	f_{DAC} = 800 MSPS, f_{OUT} = 70 MHz				87		dBc
TWO-TONE INTERMODULATION DISTORTION (IMD)	f_{DAC} = 200 MSPS, f_{OUT} = 50 MHz				91		dBc
	f_{DAC} = 400 MSPS, f_{OUT} = 60 MHz				88		dBc
	f_{DAC} = 400 MSPS, f_{OUT} = 80 MHz				81		dBc
	f_{DAC} = 800 MSPS, f_{OUT} = 100 MHz				88		dBc
NOISE SPECTRAL DENSITY (NSD)	f_{DAC} = 156 MSPS, f_{OUT} = 60 MHz				-158		dBm/Hz
	f_{DAC} = 200 MSPS, f_{OUT} = 80 MHz				-157		dBm/Hz
	f_{DAC} = 312 MSPS, f_{OUT} = 100 MHz				-159		dBm/Hz
	f_{DAC} = 400 MSPS, f_{OUT} = 100 MHz				-159		dBm/Hz
WCDMA ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER	f_{DAC} = 245.76 MSPS, f_{OUT} = 20 MHz				80		dBc
	f_{DAC} = 491.52 MSPS, f_{OUT} = 100 MHz				79		dBc
	f_{DAC} = 491.52 MSPS, f_{OUT} = 200 MHz				74		dBc
WCDMA SECOND ADJACENT CHANNEL LEAKAGE RATIO (ACLR), SINGLE CARRIER	f_{DAC} = 245.76 MSPS, f_{OUT} = 60 MHz				78		dBc
	f_{DAC} = 491.52 MSPS, f_{OUT} = 100 MHz				80		dBc
	f_{DAC} = 491.52 MSPS, f_{OUT} = 200 MHz				76		dBc

Table 3: AC Specifications

PIN FUNCTION DESCRIPTIONS

Pin No.	Name	Description	Pin No.	Name	Description
1	VDDC18	1.8 V Clock Supply	51	P2D<6>	Port 2 Data Input D6
2	VDDC18	1.8 V Clock Supply	52	P2D<5>	Port 2 Data Input D5
3	VSSC	Clock Common	53	VDDD18	1.8 V Digital Supply
4	VSSC	Clock Common	54	VSSD	Digital Common
5	CLK+	Differential Clock Input	55	P1D<4>	Port 2 Data Input D4
6	CLK-	Differential Clock Input	56	P1D<3>	Port 2 Data Input D3
7	VSSC	Clock Common	57	P1D<2>	Port 2 Data Input D2
8	VSSC	Clock Common	58	P1D<1>	Port 2 Data Input D1
9	VDDC18	1.8 V Clock Supply	59	P1D<0>	Port 2 Data Input D0 (LSB)
10	VDDC18	1.8 V Clock Supply	60	VDDD18	1.8 V Digital Supply
11	VSSC	Clock Common	61	VDDD33	3.3 V Digital Supply
12	VSSA	Analog Common	62	SYNC_O-	Differential Synchronization Output
13	SYNC_I+	Differential Synchronization Input	63	SYNC_O+	Differential Synchronization Output
14	SYNC_I-	Differential Synchronization Input	64	VSSD	Digital Common
15	VSSD	Digital Common	65	PLL_LOCK	PLL Lock Indicator
16	VDDD18	1.8 V Digital Supply	66	SPI_SDO	SPI Port Data Output
17	P1D<15>	Port 1 Data Input D15 (MSB)	67	SPI_SDIO	SPI Port Data Input/Output
18	P1D<14>	Port 1 Data Input D14	68	SPI_CLK	SPI Port Clock
19	P1D<13>	Port 1 Data Input D13	69	SPI_CSB	SPI Port Chip Select Bar
20	P1D<12>	Port 1 Data Input D12	70	RESET	Reset, active high
21	P1D<11>	Port 1 Data Input D11	71	IRQ	Interrupt Request
22	VSSD	Digital Common	72	VSSA	Analog Common
23	VDDD18	1.8 V Digital Supply	73	IPTAT	Reference Current
24	P1D<10>	Port 1 Data Input D10	74	VREF	Voltage Reference Output
25	P1D<9>	Port 1 Data Input D9	75	I120	120 μA Reference Current
26	P1D<8>	Port 1 Data Input D8	76	VDDA33	3.3 V Analog Supply
27	P1D<7>	Port 1 Data Input D7	77	VSSA	Analog Common
28	P1D<6>	Port 1 Data Input D6	78	VDDA33	3.3 V Analog Supply
29	P1D<5>	Port 1 Data Input D5	79	VSSA	Analog Common
30	P1D<4>	Port 1 Data Input D4	80	VDDA33	3.3 V Analog Supply
31	P1D<3>	Port 1 Data Input D3	81	VSSA	Analog Common
32	VSSD	Digital Common	82	VSSA	Analog Common
33	VDDD18	1.8 V Digital Supply	83	IOUT2_P	Differential DAC Current Output, Channel 2
34	P1D<2>	Port 1 Data Input D2	84	IOUT2_N	Differential DAC Current Output, Channel 2
35	P1D<1>	Port 1 Data Input D1	85	VSSA	Analog Common
36	P1D<0>	Port 1 Data Input D0 (LSB)	86	AUX2_P	Auxiliary DAC Voltage Output, Channel 2
37	DATACLK_OUT	Data Clock Output	87	AUX2_N	Auxiliary DAC Voltage Output, Channel 2
38	VDDD33	3.3 V Digital Supply	88	VSSA	Analog Common
39	TXENABLE	Transmit Enable	89	AUX1_N	Auxiliary DAC Voltage Output, Channel 1
40	P2D<15>	Port 2 Data Input D15 (MSB)	90	AUX1_P	Auxiliary DAC Voltage Output, Channel 1
41	P2D<14>	Port 2 Data Input D14	91	VSSA	Analog Common
42	P2D<13>	Port 2 Data Input D13	92	IOUT1_N	Differential DAC Current Output, Channel 1
43	VDDD18	1.8 V Digital Supply	93	IOUT1_P	Differential DAC Current Output, Channel 1
44	VSSD	Digital Common	94	VSSA	Analog Common
45	P2D<12>	Port 2 Data Input D12	95	VSSA	Analog Common
46	P2D<11>	Port 2 Data Input D11	96	VDDA33	3.3 V Analog Supply
47	P2D<10>	Port 2 Data Input D10	97	VSSA	Analog Common
48	P2D<9>	Port 2 Data Input D9	98	VDDA33	3.3 V Analog Supply
49	P2D<8>	Port 2 Data Input D8	99	VSSA	Analog Common
50	P2D<7>	Port 2 Data Input D7	100	VDDA33	3.3 V Analog Supply

Table 4: Pin Function Descriptions

PIN CONFIGURATION

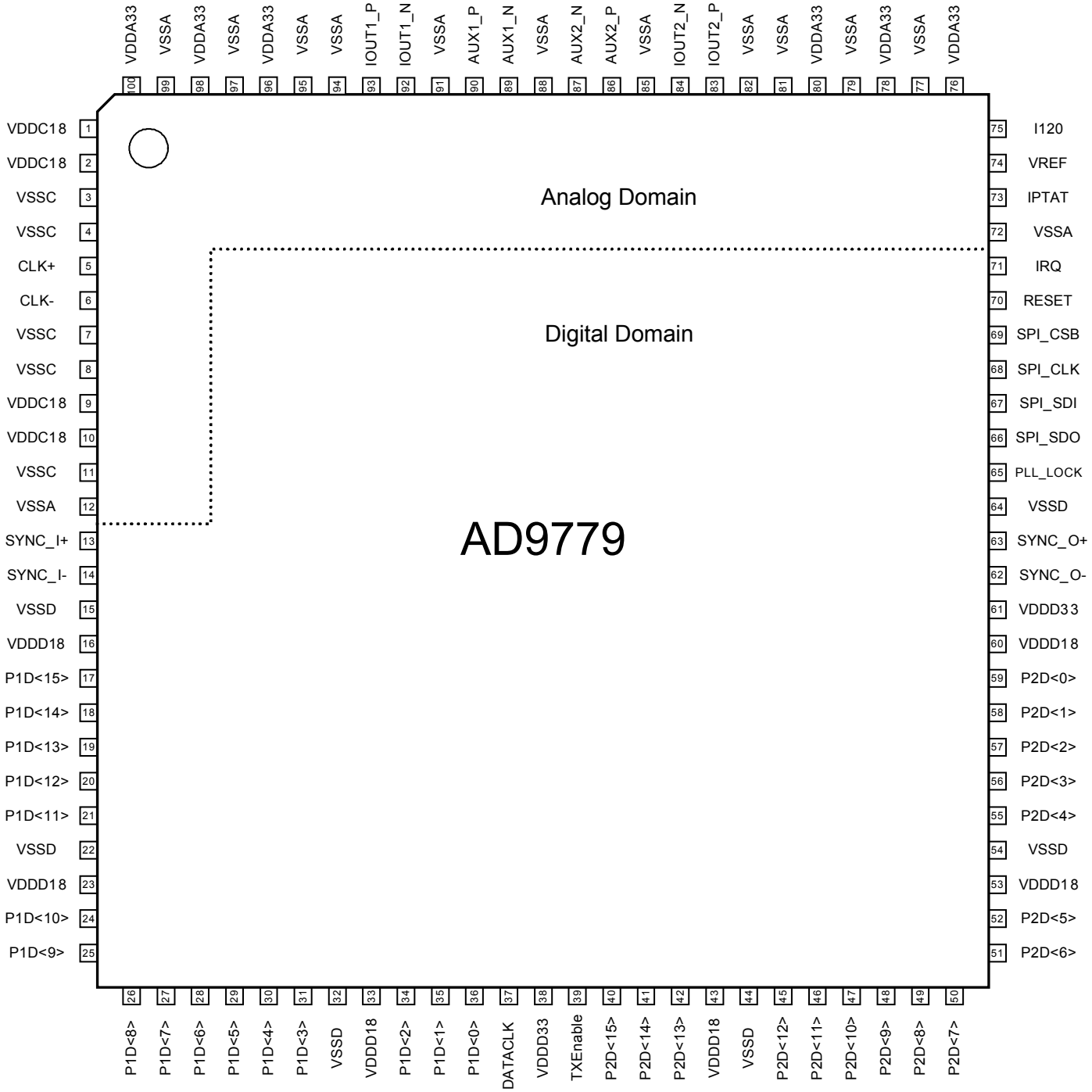


Figure 2. Pin Configuration

INTERPOLATION FILTER COEFFICIENTS

Table 5: Halfband Filter 1

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(55)	-4
H(2)	H(54)	0
H(3)	H(53)	13
H(4)	H(52)	0
H(5)	H(51)	-34
H(6)	H(50)	0
H(7)	H(49)	72
H(8)	H(48)	0
H(9)	H(47)	-138
H(10)	H(46)	0
H(11)	H(45)	245
H(12)	H(44)	0
H(13)	H(43)	-408
H(14)	H(42)	0
H(15)	H(41)	650
H(16)	H(40)	0
H(17)	H(39)	-1003
H(18)	H(38)	0
H(19)	H(37)	1521
H(20)	H(36)	0
H(21)	H(35)	-2315
H(22)	H(34)	0
H(23)	H(33)	3671
H(24)	H(32)	0
H(25)	H(31)	-6642
H(26)	H(30)	0
H(27)	H(29)	20755
H(28)		32768

Table 6: Halfband Filter 2

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(23)	-2
H(2)	H(22)	0
H(3)	H(21)	17
H(4)	H(20)	0
H(5)	H(19)	-75
H(6)	H(18)	0
H(7)	H(17)	238
H(8)	H(16)	0
H(9)	H(15)	-660
H(10)	H(14)	0
H(11)	H(13)	2530
H(12)		4096

Table 7: Halfband Filter 3

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(15)	-39
H(2)	H(14)	0
H(3)	H(13)	273
H(4)	H(12)	0
H(5)	H(11)	-1102
H(6)	H(10)	0
H(7)	H(9)	4964
H(8)		8192

Table 8: Inverse Sinc Filter

Lower Coefficient	Upper Coefficient	Integer Value
H(1)	H(9)	2
H(2)	H(8)	-4
H(3)	H(7)	10
H(4)	H(6)	-35
H(5)		401

INTERPOLATION FILTER RESPONSE CURVES

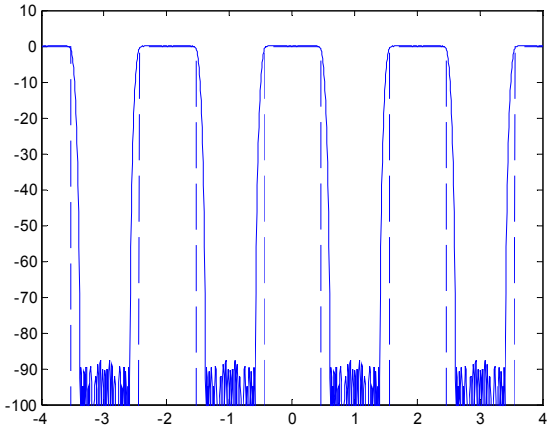


Figure 3. AD9779 2x Interpolation, Low Pass Response to ±4x Input Data Rate (Dotted Lines Indicate 1dBRoll-Off)

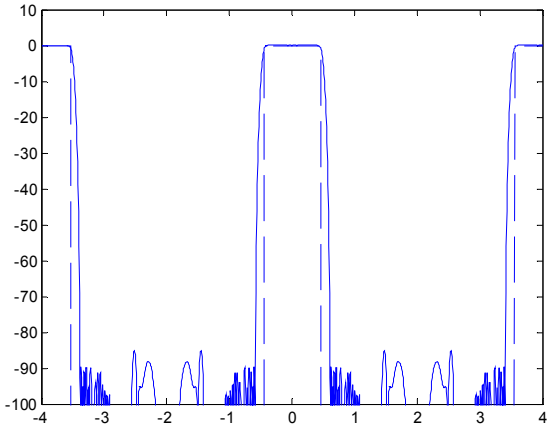


Figure 4. AD9779 4x Interpolation, Low Pass Response to ±4x Input Data Rate (Dotted Lines Indicate 1dBRoll-Off)

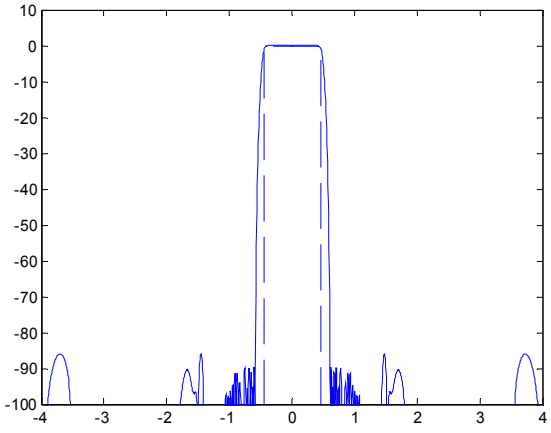


Figure 5.AD9779 8x Interpolation, Low Pass Response to ±4x Input Data Rate (Dotted Lines Indicate 1dBRoll-Off)

CHARACTERIZATION DATA

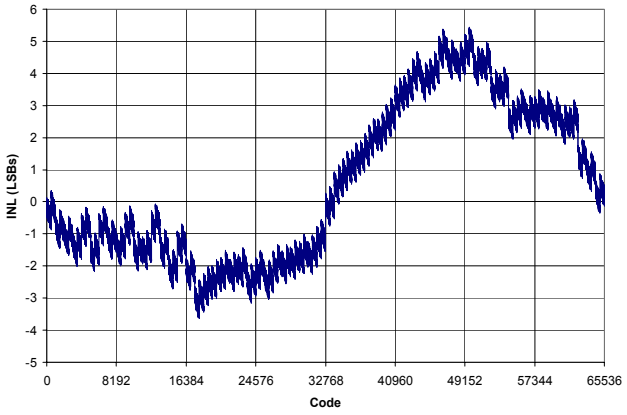


Figure 6. AD9779 Typical INL

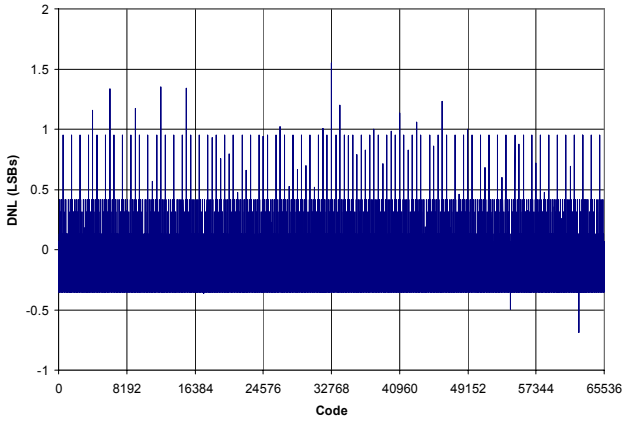


Figure 7. AD9779 Typical DNL

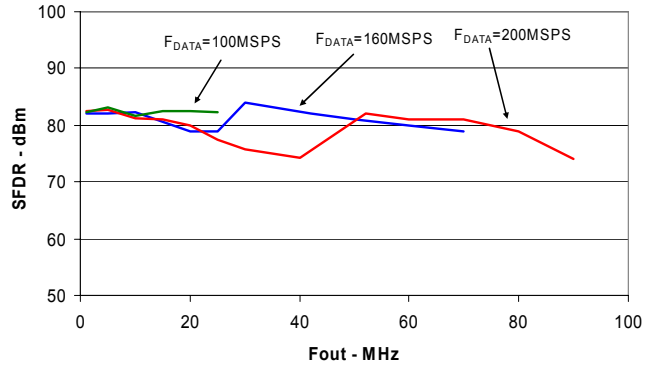


Figure 8. SFDR vs. F_{OUT}, 1x Interpolation

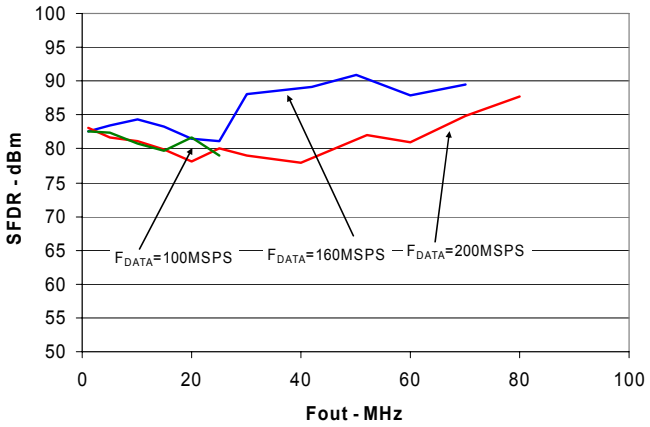


Figure 9. SFDR vs. F_{OUT}, 2x Interpolation

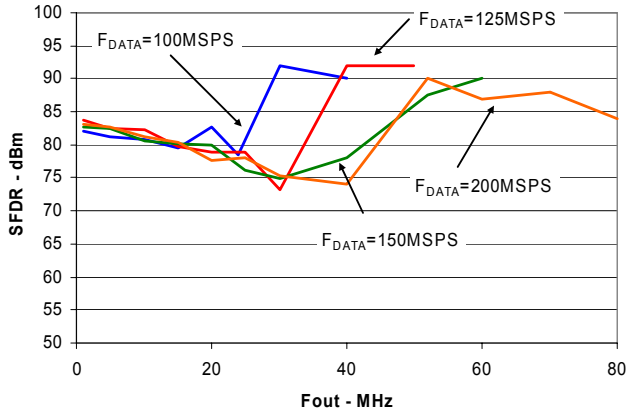


Figure 10. SFDR vs. F_{OUT}, 4x Interpolation

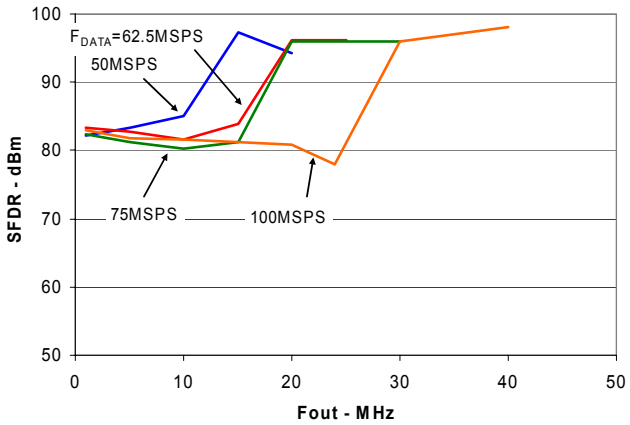


Figure 11. SFDR vs. F_{OUT}, 8x Interpolation

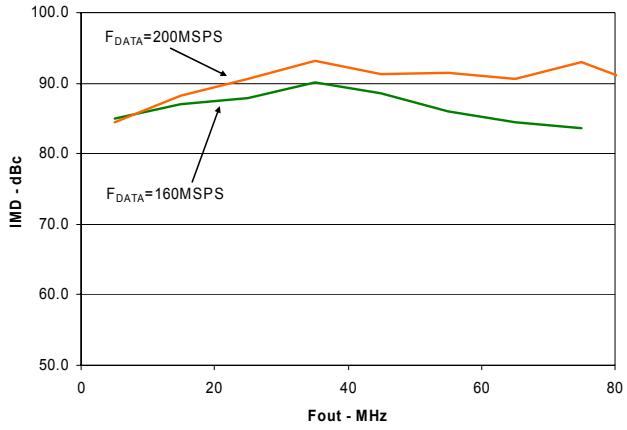


Figure 12. Third Order IMD vs. F_{OUT}, 1x Interpolation

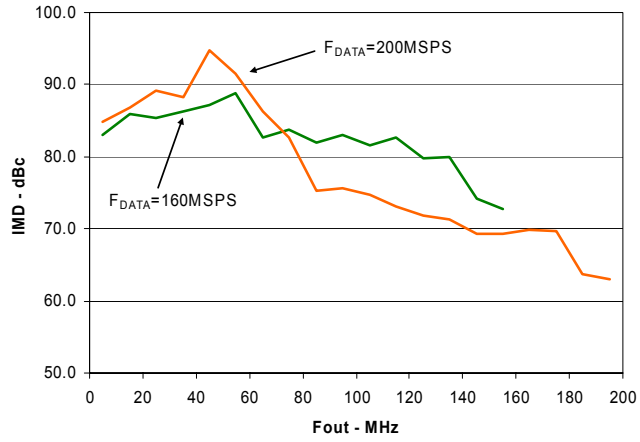


Figure 13. Third Order IMD vs. F_{OUT}, 2x Interpolation

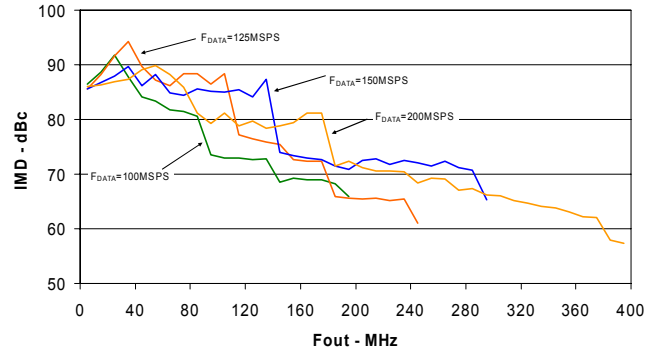


Figure 14. Third Order IMD vs. F_{OUT}, 4x Interpolation

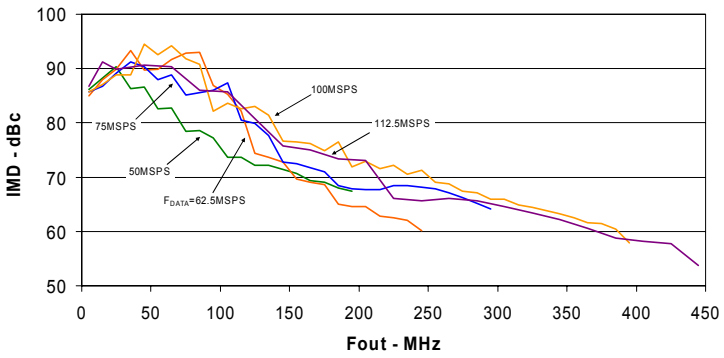


Figure 15. Third Order IMD vs. F_{OUT}, 8x Interpolation

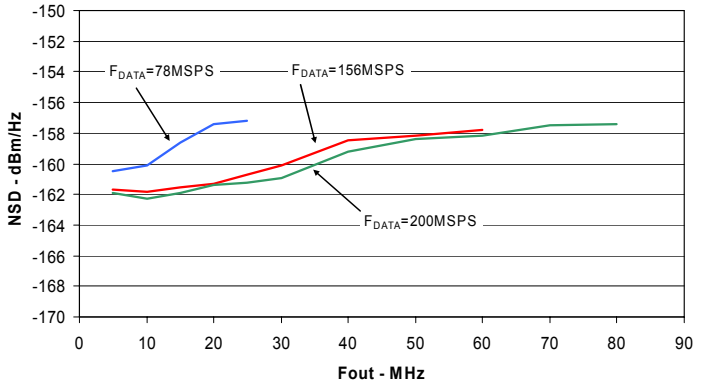


Figure 16. Noise Spectral Density vs. F_{OUT}, 1x Interpolation

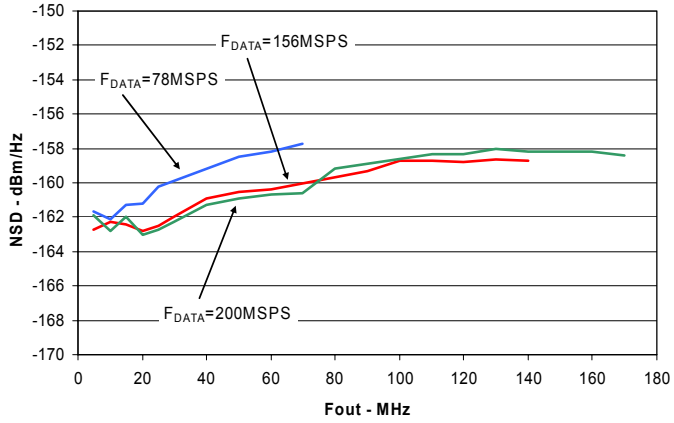


Figure 17. Noise Spectral Density vs. F_{OUT}, 2x Interpolation

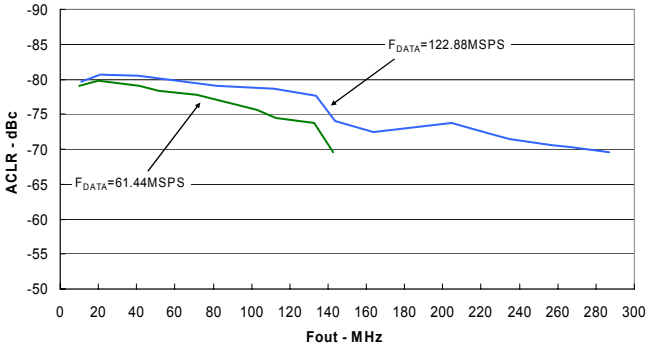


Figure 18. ACLR for 1st Adjacent Band WCDMA, 4x Interpolation. On-Chip Modulation is used to translate baseband signal to IF.

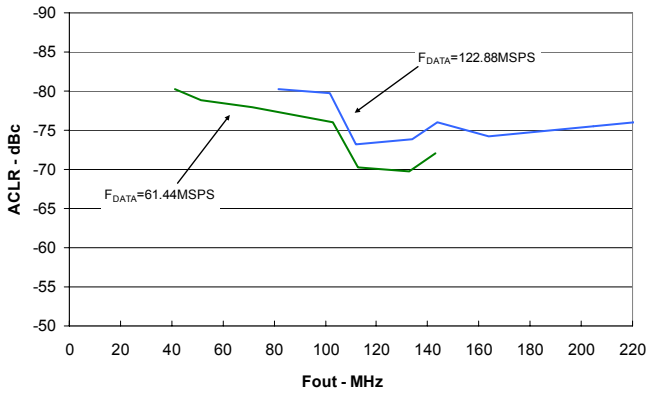


Figure 19. ACLR for 2nd Adjacent Band WCDMA, 4x Interpolation. On-Chip Modulation is used to translate baseband signal to IF.

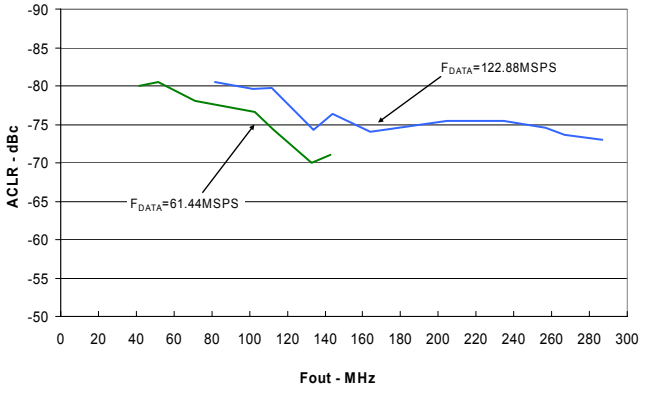


Figure 20. ACLR for 3rd Adjacent Band WCDMA, 4x Interpolation. On-Chip Modulation is used to translate baseband signal to IF.

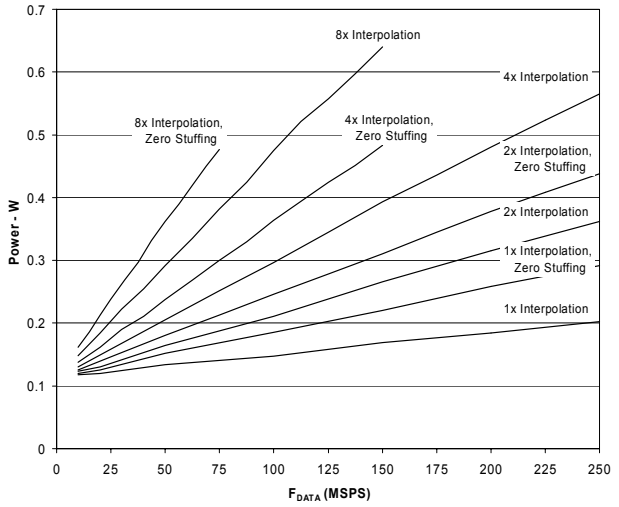


Figure 21. Power Dissipation , I Data only, Single DAC Mode

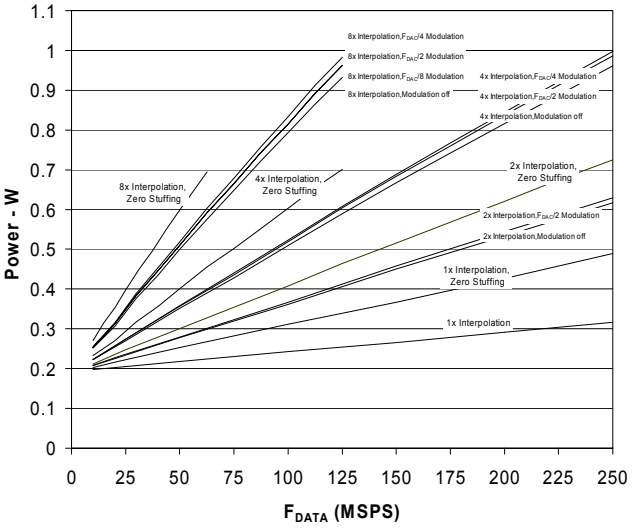


Figure 22. Power Dissipation, Dual DAC Mode

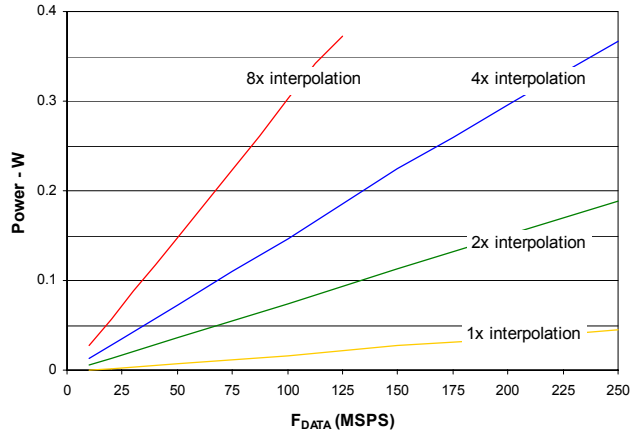


Figure 23. Power Consumption, Digital 1.8V Supply, I Data only, Real Mode, does not include zero stuffing

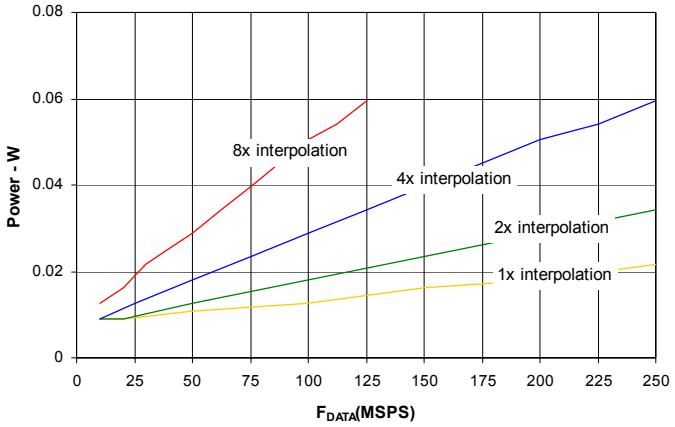


Figure 24. Power Consumption, Clock 1.8V Supply, I Data only, Single DAC Mode, includes modulation modes, does not include zero stuffing

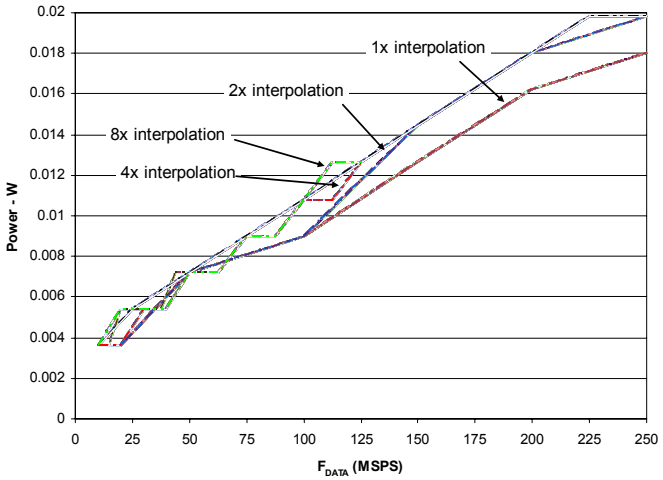


Figure 25. Digital 3.3V Supply, I Data only, Single DAC Mode, includes modulation modes and zero stuffing

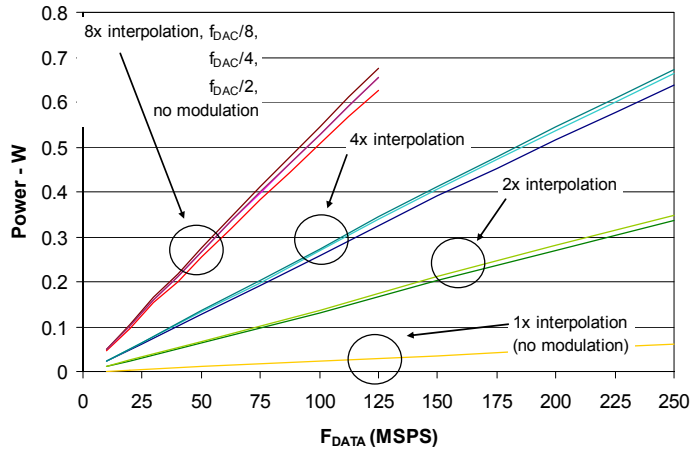


Figure 26. Power Consumption, Digital 1.8V Supply, I Data only, Dual DAC Mode, does not include zero stuffing

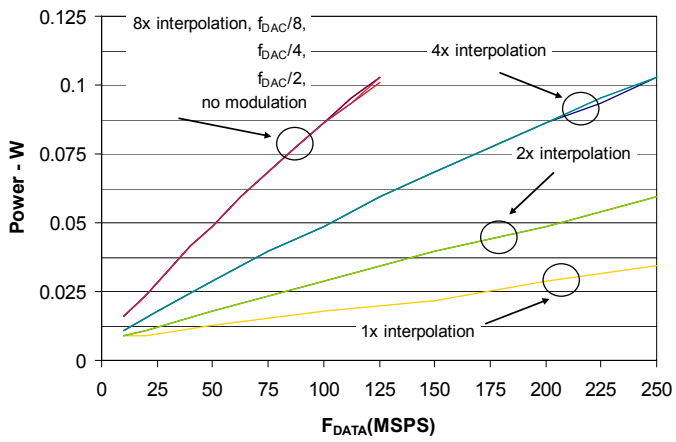


Figure 27. Power Consumption, Clock 1.8V Supply, I Data only, Dual DAC Mode, does not include zero stuffing

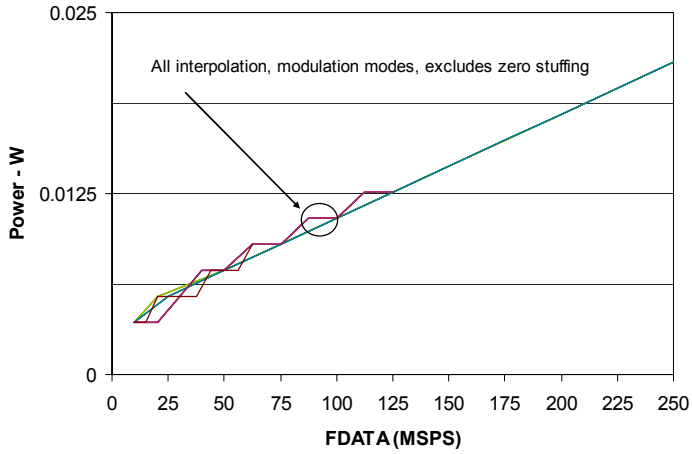


Figure 28. Digital 3.3V Supply, I Data only, Dual DAC Mode

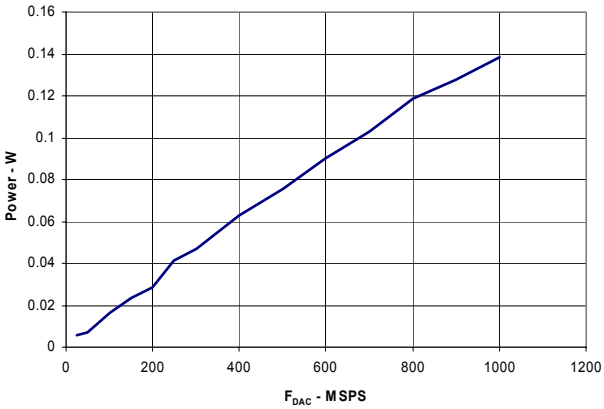


Figure 29. Power Dissipation of Inverse Sinc Filter

GENERAL DESCRIPTION

The AD9779 combines many features which make it a very attractive DAC for wired and wireless communications systems. The dual digital signal path and dual DAC structure allow an easy interface with common quadrature modulators when designing single sideband transmitters. The speed and performance of the AD9779 allow wider bandwidths/more carriers to be synthesized than with previously available DACs. The digital engine in the AD9779 uses a breakthrough filter architecture that combines the interpolation with a digital quadrature modulator. This allows the AD9779 to do digital quadrature frequency up conversion. The AD9779 also has features which allow simplified synchronization with incoming data, and also allows multiple AD9779s to be synchronized.

Serial Peripheral Interface

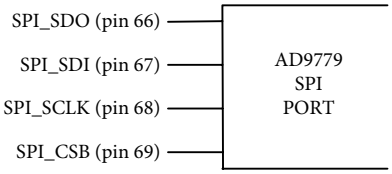


Figure 30. AD9779 SPI Port

The AD9779 serial port is a flexible, synchronous serial communications port allowing easy interface to many industry-standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola SPI® and Intel® SSR protocols. The interface allows read/write access to all registers that configure the AD9779. Single or multiple byte transfers are supported, as well as MSB first or LSB first transfer formats. The AD9779's serial interface port can be configured as a single pin I/O (SDIO) or two unidirectional pins for in/out (SDIO/SDO).

General Operation of the Serial Interface

There are two phases to a communication cycle with the AD9779. Phase 1 is the instruction cycle, which is the writing of an instruction byte into the AD9779, coincident with the first eight SCLK rising edges. The instruction byte provides the AD9779 serial port controller with information regarding the data transfer cycle, which is Phase 2 of the communication cycle. The Phase 1 instruction byte defines whether the upcoming data transfer is read or write, the number of bytes in the data transfer, and the starting register address for the first byte of the data transfer. The first eight SCLK rising edges of each communication cycle are used to write the instruction byte into the AD9779.

A logic high on the CS pin, followed by a logic low, will reset the SPI port timing to the initial state of the instruction cycle. From this state, the next 8 rising SCLK edges represents the instruction bits of the current IO operation This is true regardless of the present state of the internal registers or the other signal levels present at the inputs to the SPI port. If the SPI port is in the midst of an instruction cycle or a data transfer cycle, none of the present data will be written.

The remaining SCLK edges are for Phase 2 of the communication cycle. Phase 2 is the actual data transfer between the AD9779 and the system controller. Phase 2 of the communication cycle is a transfer of 1, 2, 3, or 4 data bytes as determined by the instruction byte. Using one multi-byte transfer is the preferred method. Single byte data transfers are useful to reduce CPU overhead when register access requires one byte only. Registers change immediately upon writing to the last bit of each transfer byte.

Instruction Byte

The instruction byte contains the information shown in *Table 9*.

MSB							LSB
I7	I6	I5	I4	I3	I2	I1	I0
R/W	N1	N0	A4	A3	A2	A1	A0

Table 9. SPI Instruction Byte

R/W, Bit 7 of the instruction byte, determines whether a read or a write data transfer will occur after the instruction byte write. Logic high indicates read operation. Logic 0 indicates a write operation.

N1, N0, Bits 6 and 5 of the instruction byte, determine the number of bytes to be transferred during the data transfer cycle. The bit decodes are shown in *Table 10*.

A4, A3, A2, A1, A0, Bits 4, 3, 2, 1, 0 of the instruction byte, determine which register is accessed during the data transfer portion of the communications cycle. For multibyte transfers, this address is the starting byte address. The remaining register addresses are generated by the AD9779 based on the LSBFIRST bit (REG00, bit 6).

N0	N1	Description
0	0	Transfer 1 Byte
0	1	Transfer 2 Bytes
1	0	Transfer 3 Bytes
1	1	Transfer 4 Bytes

Table 10. Byte Transfer Count

Serial Interface Port Pin Descriptions

SCLK—Serial Clock. The serial clock pin is used to synchronize data to and from the AD9779 and to run the internal state machines. SCLK's maximum frequency is 40 MHz. All data input to the AD9779 is registered on the rising edge of SCLK. All data is driven out of the AD9779 on the falling edge of SCLK.

CSB—Chip Select. Active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communications lines. The SDO and SDIO pins will go to a high impedance state when this input is high. Chip select should stay low during the entire communication cycle.

SDIO—Serial Data I/O. Data is always written into the AD9779 on

this pin. However, this pin can be used as a bidirectional data line. The configuration of this pin is controlled by Bit 7 of register address 00h. The default is Logic 0, which configures the SDIO pin as unidirectional.

SDO—Serial Data Out. Data is read from this pin for protocols that use separate lines for transmitting and receiving data. In the case where the AD9779 operates in a single bidirectional I/O mode, this pin does not output data and is set to a high impedance state.

MSB/LSB Transfers

The AD9779 serial port can support both most significant bit (MSB) first or least significant bit (LSB) first data formats. This functionality is controlled by register bit LSBFIRST (REG00, bit 6). The default is MSB first (LSBFIRST = 0).

When LSBFIRST = 0 (MSB first) the instruction and data bit must be written from most significant bit to least significant bit. Multi-byte data transfers in MSB first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes should follow in order from high address to low address. In MSB first mode, the serial port internal byte address generator decrements for each data byte of the multibyte communication cycle.

When LSBFIRST = 1 (LSB first) the instruction and data bit must be written from least significant bit to most significant bit. Multi-byte data transfers in LSB first format start with an instruction byte that includes the register address of the least significant data byte followed by multiple data bytes. The serial port internal byte address generator increments for each byte of the multi-byte communication cycle.

The AD9779 serial port controller data address will decrement from the data address written toward 0x00 for multi-byte I/O operations if the MSB first mode is active. The serial port controller address will increment from the data address written toward 0x1F for multi-byte I/O operations if the LSB first mode is active.

Notes on Serial Port Operation

The AD9779 serial port configuration is controlled by REG00, bits 6 and 7 . It is important to note that the configuration changes immediately upon writing to the last bit of the byte. For multi-byte transfers, writing to this register may occur during the middle of communication cycle. Care must be taken to compensate for this new configuration for the remaining bytes of the current communication cycle.

The same considerations apply to setting the software reset, RESET (REG00, bit 5). All registers are set to their default values EXCEPT REG00 and REG04 which remain unchanged.

Use of only single byte transfers when changing serial port configurations or initiating a software reset is recommended to prevent unexpected device behavior.

As described above, all serial port data is transferred to/from the AD9779 synchronous to the SCLK pin. If synchronization is lost, the AD9779 has the ability to asynchronously terminate an IO operation, putting the AD9779 serial port controller into a known state, thereby regaining synchronization.

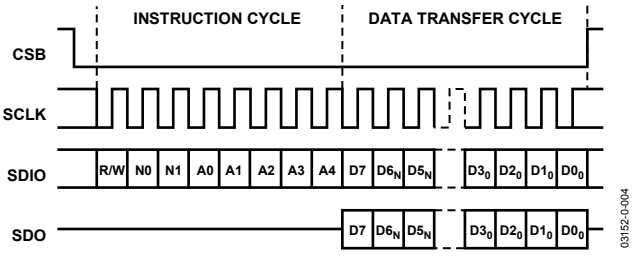


Figure 31. Serial Register Interface Timing MSB First

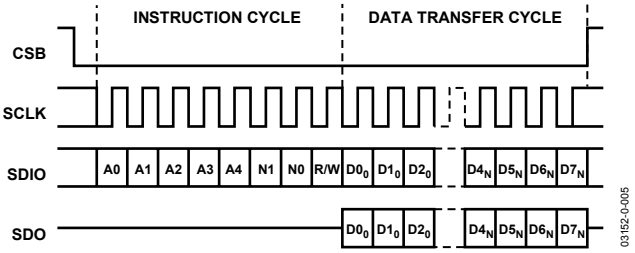


Figure 32. Serial Register Interface Timing LSB First

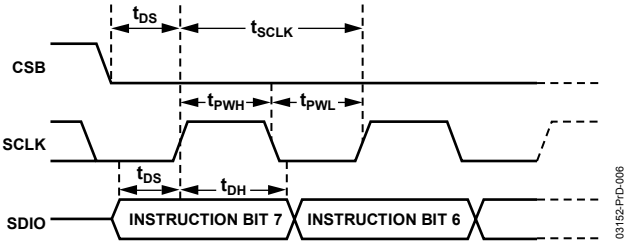


Figure 33. Timing Diagram for SPI Register Write

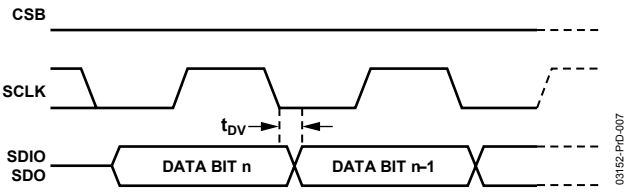


Figure 34. Timing Diagram for SPI Register Read

SPI Register Map

Register Name	Address		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default
Comm Register	00h	00	SDIO Bidirectional	LSB,MSB First	Software Reset	Power Down Mode	Auto Power Down Enable		PLL Lock Indicator		00h
Digital Control Register	01h	01	Filter Interpolation Factor <1: 0>		Filter Modulation Mode <3:0>					Zero Stuffing Enable	00h
	02h	02	Data Format	Single/Interleaved Data Bus Mode	Real Mode	Data Clock Delay Enable	Inverse Sinc Enable	DATACLK Invert	TxEnable / IQ Select Invert	Q First	00h
Sync Control Register	03h	03	Data Clock Delay Mode <1:0>		Extra Data Clock Divide Ratio<1:0>		Input Data Timing Error Tolerance <3:0>				00h
	04h	04	Data Clock Delay <3:0>				Output Sync Pulse Divide <2:0>			Sync Out Delay <4>	00h
	05h	05	Sync Out Delay <3:0>				Input Sync Pulse Frequency			Sync Input Delay <4>	00h
	06h	06	Sync Input Delay <3:0>				Input Sync Pulse Timing Error Tolerance <3:0>				00h
	07h	07	Sync Receiver Enable	Sync Driver Enable	Sync Triggering Edge	Sync_I to Input Data Sampling Clock Offset <4:0>					00h
PLL Control	08h	08	PLL Band Select <5:0>						PLL VCO AGC Gain <1:0>		CFh
	09h	09	PLL Enable	PLL VCO Divider Ratio <1:0>		PLL Loop Divide Ratio <1:0>		PLL Bias Setting <2:0>			37h
Misc. Control Register	0Ah	10	PLL Control Voltage Range <2:0>			PLL Loop Bandwidth Adjustment <4:0>					38h

I DAC Control Register	0Bh	11	IDAC Gain Adjustment <7:0>							F9h
	0Ch	12	IDAC SLEEP	IDAC Power Down					IDAC Gain Adjustment <9:8>	01h
Aux 1 DAC Control Register	0Dh	13	Auxiliary DAC1 Data <7:0>							00h
	0Eh	14	Auxiliary DAC1 Sign	Auxiliary DAC1 Current Direction	Auxiliary DAC1 Power Down				Auxiliary DAC1 Data <9:8>	00h
Q DAC Control Register	0Fh	15	QDAC Gain Adjustment <7;0>							F9h
	10h	16	QDAC SLEEP	QDAC Power Down					QDAC Gain Adjustment <9:8>	01h
Aux 2 DAC Control Register	11h	17	Auxiliary DAC2 Data <7:0>							00h
	12h	18	Auxiliary DAC2 Sign	Auxiliary DAC2 Current Direction	Auxiliary DAC2 Power Down				Auxiliary DAC2 Data <9:8>	00h
Interrupt Register	19h	25	Data Delay IRQ	Sync Delay IRQ	Cross Control IRQ		Data Delay IRQ Enable	Sync Delay IRQ Enable	Cross Control IRQ Enable	Internal Sync Loopback	00h

Table **11:** SPI Register Map

Register (hex)	Address		Name	Function	Default
Comm Register	00	7	SDIO Bidirectional	0: Use SDIO pin as input data only 1: Use SDIO as both input and output data	0
	00	6	LSB/MSB First	0: First bit of serial data is MSB of data byte 1: First bit of serial data is LSB of data byte	0
	00	5	Software RESET	Bit must be written with a 1, then 0 to soft reset SPI register map	0
	00	4	Power Down Mode	0: All circuitry is active 1: Disable all digital and analog circuitry, only SPI port is active	0
	00	3	Auto Power Down Enable	Controls power down model, see page 23 for details	0
	00	1	PLL LOCK (read only)	0: PLL is not locked 1: PLL is locked	0
Digital Control Register	01	7:6	Filter Interpolation Factor	00: 1× interpolation 01: 2× interpolation 10: 4× interpolation 11: 8× interpolation	00
	01	5:2	Filter Modulation Mode	See Table 13 for filter modes	0000
	01	0	Zero Stuffing	0: Zero stuffing off 1: Zero stuffing on	0
	02	7	Data Format	0: Signed binary 1: Unsigned binary	0
	02	6	Dual/ Interleaved Data Bus Mode	0: Both input data ports receive data 1: Data port 1 only receives data	0
	02	5	Real Mode	0: Enable Q path for signal processing 1: Disable Q path data (internal Q channel clocks disabled, I and Q modulators disabled)	0
	02	3	Inverse Sinc Enable	0: Inverse sinc disabled 1: Inverse sinc enabled	0
	02	2	DATACLK Invert	0: Output DATACLK same phase as internal capture clock 1: Output DATACLK opposite phase as internal capture clock	0
	02	1	TxEnable Invert	Inverts the function of TxEnable pin 39. More details on page 23.	0
	02	0	Q First	0: First byte of data is always I data at beginning of transmit 1: First byte of data is always Q data at beginning of transmit	
Sync Control Register	03	7:6	Data Clock Delay Mode	00: Manual, no error correction 01: Manual error correction 10: automatic, one pass check 11: automatic, continuous pass check	00
	03	5:4	Extra Data Clock Divide Ratio	Data Clock Output Divider	000
	03	3:0	Input Data Timing Error Tolerance	Input data window delay control, see page 28 for details.	000
	04	7:4	Data Clock Delay	Sets delay of DACCLK in to DATACLK out	0000
	04	3:1	Output Sync Pulse Divide	Sets frequency of Sync_Out pulses	0000
	04	0	Sync Out Delay	Sync Output Delay, bit 4	
	05	7:4	Sync Out Delay	Sync Output Delay, <3:0>	0
	05	3:1	Input Sync Pulse Frequency	Input Sync Pulse Frequency Divider	0
	05	0	Sync Input Delay	Sync Input Delay, bit 4	0

Sync Control Register	06	7:4	Sync Input Delay		0
	06	3:0	Input Sync Pulse Timing Error Tolerance		0
	07	7	Sync Receiver Enable		0
	07	6	Sync Driver Enable		0
	07	5	Sync Triggering Edge		0
	07	4:0	Sync_I to input data sampling clock offset		0
PLL Control	08	7:2	PLL Band Select	See Table 14. VCO Frequency Range vs. PLL Band Select Value	110011
	08	1:0	VCO AGC Gain Control	Lower number (low gain) is generally better for performance.	11
	09	7	PLL Enable	0: PLL off, DAC rate clock supplied by outside source 1: PLL on, DAC rate clock synthesized internally from data rate clock via PLL clock multiplier	10
	09	6:5	PLL VCO Divide Ratio	FVCO/FDAC: 00 ×1 01 ×2 10 ×4 11 ×8	
	09	4:3	PLL Loop Divide Ratio	FDAC/FREF: 00 ×2 01 ×4 10 ×8 11 ×16	
	09	2:0	PLL Bias Setting		111
Misc. Control	0A	7:5	PLL Control Voltage Range	000 to 111, higher number means higher control voltage	
	0A	4:0	PLL Loop Bandwidth Adjustment	See page 21 for description	
IDAC Control Register	0B	7:0	IDAC Gain Adjustment	(7:0) LSB slice of 10 bit gain setting word for IDAC	11111001
	0C	7	IDAC Sleep	0: IDAC on 1: IDAC off	0
	0C	6	IDAC Power Down	0: IDAC on 1: IDAC off	0
	0C	1:0	IDAC Gain Adjustment	(9:8) MSB slice of 10 bit gain setting word for IDAC	01
Aux DAC 1 Control Register	0D	7:0	Aux DAC1 Gain Adjustment	(7:0) LSB slice of 10 bit gain setting word for Aux DAC1	00000000
	0E	7	Aux DAC1 Sign	0: Positive 1: Negative	
	0E	6	Aux DAC1 Current Direction	0: Source 1: Sink	0
	0E	5	Aux DAC1 Power Down	0: Aux DAC1 on 1: Aux DAC 1 off	0
	0E	1:0	Aux DAC1 Gain Adjustment	(9:8) MSB slice of 10 bit gain setting word for Aux DAC1	00

QDAC Control Register	0F	7:0	QDAC Gain Adjustment	(7:0) LSB slice of 10 bit gain setting word for QDAC	11111001
	10	7	QDAC Sleep	0: QDAC on 1: QDAC off	0
	10	6	QDAC Power Down	0: QDAC on 1: QDAC off	0
	10	1:0	Aux DAC 2 Gain Adjustment	(9:8) MSB slice of 10 bit gain setting word for Aux DAC 2	
Aux DAC 2 Control Register	11	7:0	Aux DAC 2 Gain Adjustment	(7:0) LSB slice of 10 bit gain setting word for Aux DAC 2	00000000
	12	7	Aux DAC 2 Sign	0: Positive, 1: Negative	
	12	6	Aux DAC 2 Current Direction	0: Source 1: Sink	0
	12	5	Aux DAC 2 Power Down	0: Aux DAC 2 on 1: Aux DAC 2 off	0
	12	1:0	Aux DAC 2 Gain Adjustment	(9:8) MSB slice of 10 bit gain setting word for Aux DAC2	00
Interest Register	19	7	Data Delay IRQ		0
	19	6	Sync Delay IRQ		0
	19	5	Cross Control IRQ		0
	19	3	Data Delay IRQ Enable		0
	19	2	Sync Delay IRQ Enable		0
	19	1	Cross Control IRQ Enable		0
	19	0	Internal Sync Loopback		0

Table 12: SPI RegisterDescription

Interp. Factor <7:6>	Filter Mode <5:2>	Modulation	Nyquist Zone Passband	F_low	Center	F_High	
				(Freq. Normalized to F_{DAC})			
8	00h	DC_odd	1	-0.05	0	0.05	In 8x interpolation; BW(min) = 0.0375*FDAC BW(max) = 0.1*FDAC
8	01h	DC_even	2	0.0125	0.0625	0.1125	
8	02h	F/8_odd	3	0.075	0.125	0.175	
8	03h	F/8_even	4	0.1375	0.1875	0.2375	
8	04h	2F/8_odd	5	0.2	0.25	0.3	
8	05h	2F/8_even	6	0.2625	0.3125	0.3625	
8	06h	3F/8_odd	7	0.325	0.375	0.425	
8	07h	3F/8_even	8	0.3875	0.4375	0.4875	
8	08h	-4F/8_even	-8	-0.55	-0.5	-0.45	
8	09h	-4F/8_odd	-7	-0.4875	-0.4375	-0.3875	
8	0Ah	-3F/8_even	-6	-0.425	-0.375	-0.343	
8	0Bh	-3F/8_odd	-5	-0.3625	-0.3125	-0.2625	
8	0Ch	-2F/8_even	-4	-0.3	-0.25	-0.2	
8	0Dh	-2F/8_odd	-3	-0.2375	-0.1875	-0.1375	
8	0Eh	-F/8_even	-2	-0.175	-0.125	-0.075	
8	0Fh	-F/8_odd	-1	-0.1125	-0.0625	-0.0125	
4	00h	DC_odd	1	-0.1	0	0.1	In 4x interpolation; BW(min) = 0.075*FDAC BW(max) = 0.2*FDAC
4	01h	DC_even	2	0.025	0.125	0.225	
4	02h	F/4_odd	3	0.15	0.25	0.35	
4	03h	F/4_even	4	0.275	0.375	0.475	
4	04h	-F/2_even	-4	-0.6	-0.5	-0.4	
4	05h	-F/2_odd	-3	-0.475	-0.375	-0.275	
4	06h	-F/4_even	-2	-0.35	-0.25	-0.15	
4	07h	-F/4_odd	-1	-0.225	-0.125	-0.025	
2	00h	DC_odd	1	-0.2	0	0.2	In 2x interpolation; BW(min) = 0.15*FDAC BW(max) = 0.4*FDAC
2	01h	DC_even	2	0.05	0.25	0.45	
2	02h	-F/2_even	-1	-0.7	-0.5	-0.3	
2	03h	-F/2_odd	-2	-0.45	-0.25	-0.05	

Table 13: Interpolation Filter Modes, see Reg 01, bits 5 :2

PLL Frequency Band Select	
PLL Band Select Value	Frequency Band in MHz
111111 (63)	Auto
111110 (62)	2038-2170
111101 (61)	1984-2115
111100 (60)	1965-2094
111011 (59)	1947-2077
111010 58)	1931-2059
111001 (57)	1910-2038
111000 (56)	1891-2018
110111 (55)	1877-2005
110110 (54)	1856-1982
110101 (53)	1837-1962
110100 (52)	1826-1950
110011 (51)	1802-1926
110010 (50)	1781-1906
110001 (49)	1774-1896
110000 (48)	1750-1874
101111 (47)	1734-1856
101110 (46)	1725-1843
101101 (45)	1702-1822
101100 (44)	1688-1808
101011 (43)	1677-1792
101010 (42)	1646-1763
101001 (41)	1630-1741
101000 (40)	1602-1712
100111 (39)	1586-1693
100110 (38)	1560-1669
100101 (37)	1544-1646
100100 (36)	1518-1621
100011 (35)	1502-1600
100010 (34)	1478-1578
100001 (33)	1462-1557
100000 (32)	1435-1534
011111 (31)	1422-1515
011110 (30)	1397-1494
011101 (29)	1384-1477
011100 (28)	1357-1453
011011 (27)	1344-1437
011010 (26)	1318-1413
011001 (25)	1306-1397
011000 (24)	1283-1376
010111 (23)	1269-1358
010110 (22)	1246-1339
010101 (21)	1232-1318
010100 (20)	1176-1261
010011 (19)	1197-1280
010010 (18)	1144-1226
010001 (17)	1165-1245
010000 (16)	1142-1208
001111 (15)	1131-1208
001110 (14)	1109-1189
001101 (13)	1101-1176
001100 (12)	1080-1155
001011 (11)	1069-1142
001010 (10)	1050-1123
001001 (9)	1040-1110
001000 (8)	1021-1094
000111 (7)	1010-1080
000110 (6)	992-1064
000101 (5)	982-1050
000100 (4)	955-1021
000011 (3)	928-994
000010 (2)	902-966
000001 (1)	878-941
000000 (0)	854-915

Table 14. VCO Frequency Range vs. PLL Band Select Value

VCO Frequency Ranges

Because the PLL band covers greater than a 2x frequency range, the user may find themselves with two options for PLL band select, one at the lower end of the range and one at the higher end of the range. Under these conditions, VCO phase noise will be optimal when the user selects the band select value corresponding to the higher end of the frequency range. Figure 35 shows how the VCO bandwidth as well as the optimal VCO frequency varies with the band select value.

PLL Loop Filter Bandwidth

The loop filter bandwidth of the PLL is programmed via SPI reg 0A, bits 4:0. Changing these values switches capacitors on the internal loop filter. No external loop filter components are required. This loop filter has a pole at zero (P1), and then a zero (Z1)-pole (P2) combination. Z1 and P2 occur within a decade of each other. The location of this zero-pole is determined by bit 4:0. For a setting of 00000, the pole-zero occurs near 10MHz. By setting bits 4:0 to 11111, the Z1/P2 combination can be lowered to approximately 1MHz. The relationship between bits 4:0 and the position of the pole-zero between 1MHz and 10MHz is linear. The internal

components are not low tolerance, however, and can drift by as much as ±30 %.

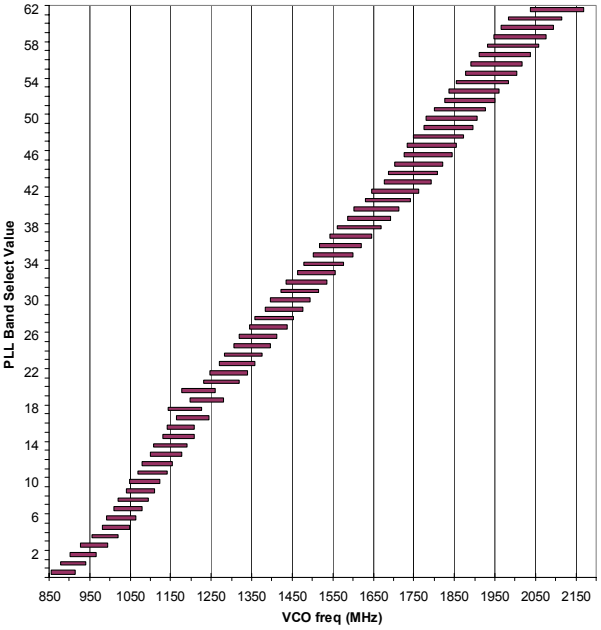


Figure 35. PLL Band Select vs. Frequency

Internal Reference/Full Scale Current Generation

Full scale current on the AD9779 IDAC and QDAC can be set from 10 to 30ma. Initially, the 1.2V bandgap reference is used to set up a current in an external resistor connected to I120 (pin 75). A simplified block diagram of the AD9779 reference circuitry is given below in Figure 36. The recommended value for the external resistor is 10k Ω, which sets up an I REFERENCE in the resistor of 120µa which in turn provides a DAC output full scale current of 20mA. Because the gain error is a linear function of this resistor, a high precision resistor will improve gain matching to the internal matching spec of the AD9779. Internal current mirrors provide a current gain scaling, where IDAC or QDAC gain is a 10 bit word in the SPI port register (registers 0A, 0B, 0E, and 0F). The default value for the DAC gain registers gives an I_{FS} of 20mA.

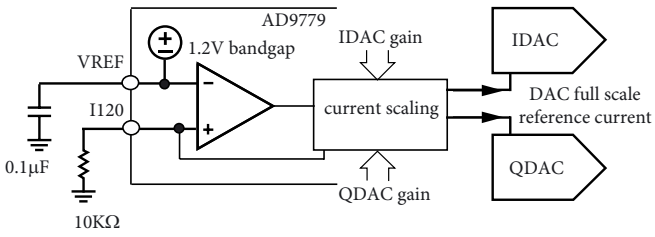


Figure 36 . Reference Circuitry

where I_{FS} is equal to;

$$\frac{1.2V}{R} \times \left(\frac{27}{12} + \left(\frac{6}{1024} \times \text{DAC gain} \right) \right) \times 32$$

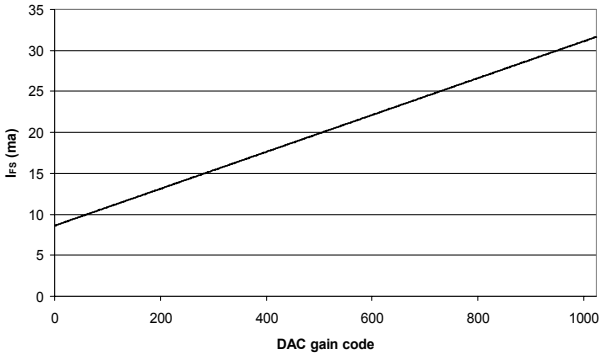


Figure 37. I_{FS} vs. DAC Gain Code

Auxiliary DACs

Two auxiliary DACs are provided on the AD9779. The full scale output current on these DACs is derived from the 1.2V bandgap reference and external resistor. The gain scale from the reference amplifier current I REFERENCE to the aux DAC reference current is 16.67 with the aux DAC gain set to full scale (10 bit values, SPI reg 0C, 0D, 10, 11), this gives a full scale current of 2ma for aux DAC1 and for aux DAC2. The aux DAC outputs are not differential. Either the P or the N side of the aux DAC is turned on at one time, with the other acting as a high impedance (>100kΩ). In addition, the P or N outputs can act as current sources or sinks. This control of P and N for both aux DACs via registers 0Eh and 10h, bits 7:6. When sourcing current, the output compliance voltage is 0-1.5V, and when sinking current the output compliance voltage is 0.8-1.5V.

The Aux DACs can be used for LO cancellation when the DAC output is followed by a quadrature modulator. A typical DAC to Quadrature Modulator interface is given in *Figure 38*. Often, the input common mode voltage for the modulator is much higher than the output compliance range of the DAC, so that ac coupling is necessary. If the required common mode input voltage on the quadrature modulator matches that of the DAC, then the ac coupling capacitors can be removed. The input referred dc offset voltage of the quadrature modulator (as well as the DAC output offset voltage mismatch) can result in LO feedthrough on the modulator output, degrading system performance. If the configuration of *Figure 38* is used, the Aux DACs can be used to compensate for this dc offset, thus reducing LO feedthrough. A lowpass or bandpass filter is recommended when spurious signals from the DAC (distortion, DAC images) at the quadrature modulator inputs may affect the system performance. This filter should be placed at the quadrature modulator inputs.

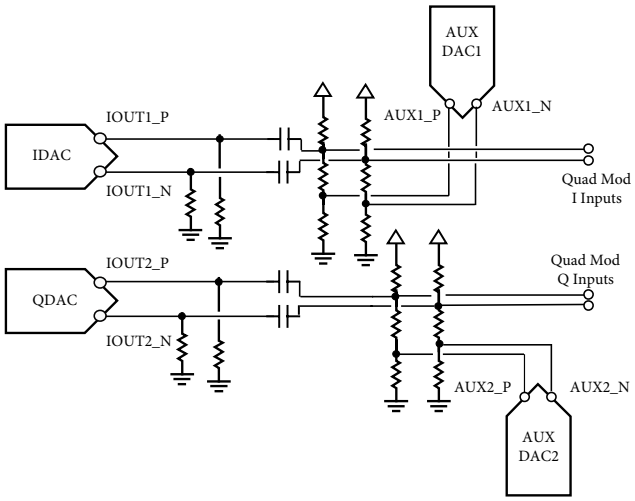


Figure 38. Typical Use of Auxiliary DACs

Power Dissipation

Figure 21 through Figure 29 show the power dissipation of the 1.8V and 3.3V digital and clock supplies in single DAC and dual DAC modes. In addition to this, the power dissipation/current of the 3.3V supply (mode and speed independent) in single DAC mode is 102mW/31mA. In Dual DAC mode, this is 182mW/51mA.

Power Down and Sleep Modes

The AD9779 has a variety of power down modes, so that the digital engine, main TxDACs, or auxiliary DACs can be powered down individually, or all at once. Via the SPI port, the main TxDACs can be placed in sleep or power down modes. In sleep mode, the TxDAC output is turned off, thus reducing power dissipation. The reference remains powered on though, so that recovery from sleep mode is very fast. With the power down mode bit set (register 00h, bit 4), all analog and digital circuitry, including the reference, are powered down. The SPI port remains active in this mode. This mode offers more substantial power savings than in sleep mode, but the time to turn on is much longer. The Auxiliary DACs also have the capability to be programmed via the SPI port into sleep mode.

The auto power down enable bit (register 00h, bit 3) controls the power down function for the digital section of the AD9779. The auto power down function works in conjunction with the TxEnable pin (pin 39) according to the following;

TxEnable (pin 39) =
0: auto power down enable =
0: Flush data path with zeroes
1: Flush data for multiple DACCLK cycles, then automatically place digital engine in power down state, DACs, reference, and SPI port are not affected.
1: Normal operation

The TxEnable bit is dual function. In dual port mode, it is simply used to power down the digital section of the AD9779. In interleaved mode, the IQ data stream is synchronized to the rising edge of TxEnable. That is, to achieve IQ synchronization, TxEnable should be held low until an I data word is present at the inputs to data port one. A rising edge of TxEnable will now synchronize the I Q data into the AD9779. TxEnable can remain high and the input IQ data will remain synchronized. To be backwards compatible with previous DACs from ADI, such as the AD9777 and AD9786, the user can also toggle TxEnable once during each data input cycle, thus continually updating the synchronization. If TxEnable is brought low and held low for multiple DACCLK cycles, then the AD9779 will flush the data in the interpolation filters, and will shut down the digital engine after the filters are flushed. The amount of DACCLK cycles it takes for the AD9779 to go into this power down mode is then a function of the length of the equivalent 2×, 4×, or 8× interpolation filter. The timing of TxEnable, I/Q Select and filter flush and digital power down are given in

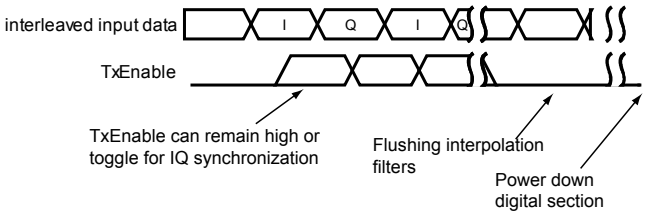


Figure 39. AD9779 TxEnable Function

The TxEnable function can be inverted by changing the status of reg 02h bit 1.

Internal PLL Clock Multiplier / Clock Distribution

The internal clock structure on the AD9779 allows the user to drive the differential clock inputs with a clock at 1x or an integer multiple of the input data rate, or at the DAC output sample rate. A PLL internal to the AD9779 provides input clock multiplication and provides all of the internal clocks required for the interpolation filters and data synchronization.

The internal clock architecture is shown in Figure 40. The reference clock is the differential clock at pins 5 and 6. This clock input can be run differentially, or singled ended by driving pin 5 with a clock signal, and biasing pin 6 to the mid swing point of the signal at pin 5. There are various configurations in which this clock architecture can be run;

1. PLL Enabled (reg 09h, bit 7=1) – The PLL enable switch in Figure 40 is connected to the junction of the dividers N1 (PLL VCO Divide Ratio) and N2 (PLL Loop Divide Ratio). Divider N3 determines the interpolation rate of the DAC, and the ratio N3/N2 determines the ratio of Reference Clock/Input Data Rate. The VCO runs optimally over the range 1.0GHz to 2.0GHz, so that N1 is used to keep the speed of the VCO in this range, even though the DAC sample rate may be lower. The loop filter components are entirely internal and no external compensation is necessary.
2. PLL Disabled (reg 09h, bit 7=0) – The PLL enable switch in Figure 40 is connected to the Reference Clock Input.

The differential reference clock input will be the DAC output sample rate and N3 will determine the interpolation rate.

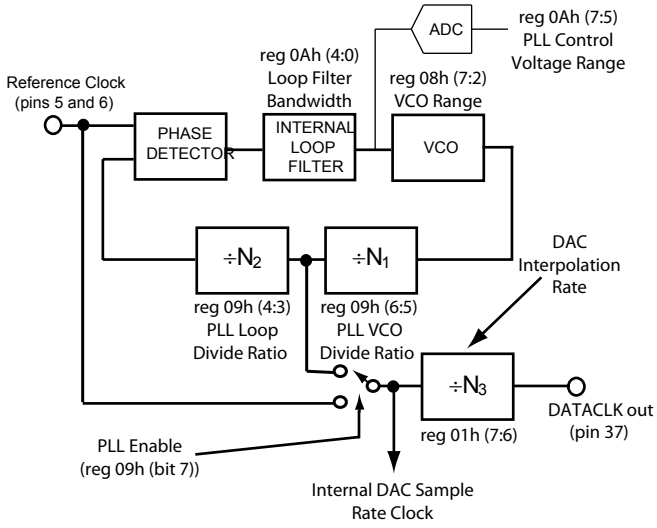


Figure 40. Internal Clock Architecture of AD9779

Timing Information

Figure 41 through Figure 43 show some of the various timing possibilities when the PLL is enabled. The combination of the settings of N2 and N3 means that the reference clock frequency may be a multiple of the actual input data rate. Figure 41 through Figure 43 show, respectively, what the timing looks like when N2/N3 = 1, and 2.

Figure 43 shows the timing specifications for the AD9779 when the PLL is disabled. The reference clock is at the DAC output sample rate. In the example shown in Figure 43, if the PLL is disabled, the interpolation is 4x.. The set up and hold time for the input data are with respect to the rising edge of DATACLK out. Note that if reg 02h, bit2 is set, DATACLK out is inverted so the latching clock edge will be the DATACLK out falling edge.

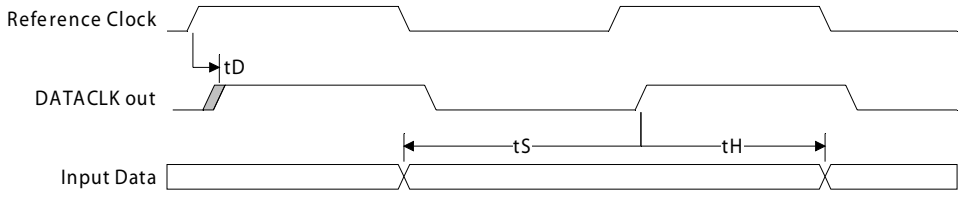


Figure 41. Timing Specifications for AD9779, PLL Enabled, Reference Clock = 1x Input Sample Rate[1]

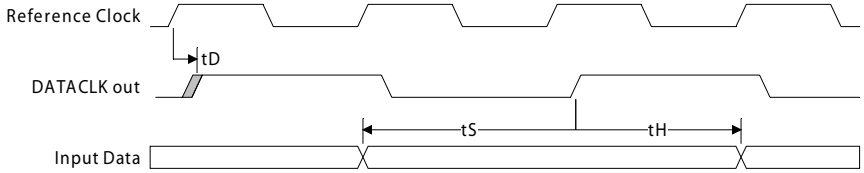
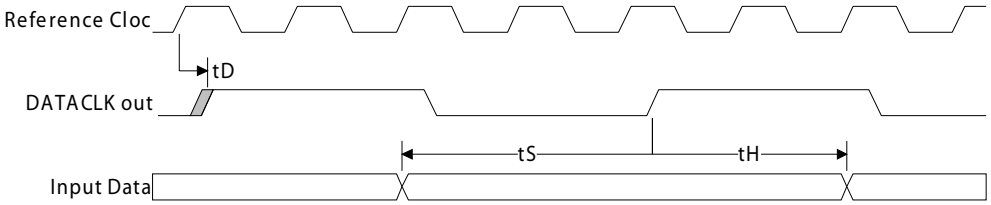


Figure 42. Timing Specifications for AD9779, PLL Enabled, Reference Clock = 2x Input Sample Rate[1]



tS= 3.2n s min
tH= - 1.6n s min
tD=5.0ns typ
(DATACLK DELAY disabled)

Figure 43. Timing Specifications for AD9779, PLL Disabled, 4x Interpolation[1]

[1] For an in depth description of how TxDAC timing specifications are specified, please read Analog Devices, application note AN748, Set up and Hold Measurements in High Speed CMOS Input DACs.

Interpolation Filter Architecture

The AD9779 can provide up to 8× interpolation or disable the interpolation filters entirely. The coefficients of the low pass filters and the inverse sinc filter are given in Table 5, Table 6, Table 7, and Table 8. Spectral plots for the filter responses are given in Figure 3, Figure 4, and Figure 5.

With the interpolation filter and modulator combined, the incoming signal can be placed anywhere within the Nyquist region of the DAC output sample rate. Where the input signal is complex, this architecture allows modulation of the input signal to positive or negative Nyquist regions (refer to Table 13).

The Nyquist regions up to 4× the input data rate can be seen in Figure 44.

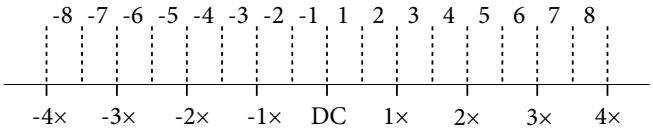


Figure 44. Nyquist Zones

Figure 3, Figure 4 and Figure 5 show the low pass response of the digital filters with no modulation used. By turning on the modulation feature, the response of the digital filters can be tuned to any Nyquist zone within the DAC bandwidth. As an example, Figure 45 to Figure 51 show the odd mode filter responses (refer to Table 13 for odd/even mode filter responses).

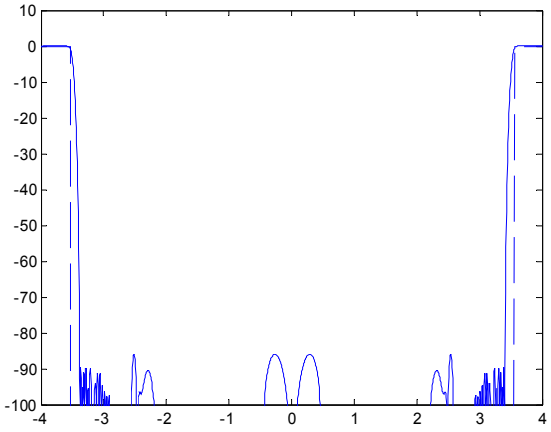


Figure 45. Interpolation/Modulation Combination of -4f_{DAC}/8 Filter in Odd Mode

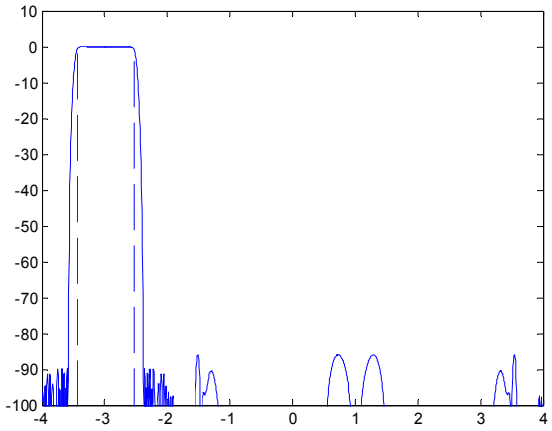


Figure 46. Interpolation/Modulation Combination of -3f_{DAC}/8 Filter in Odd Mode

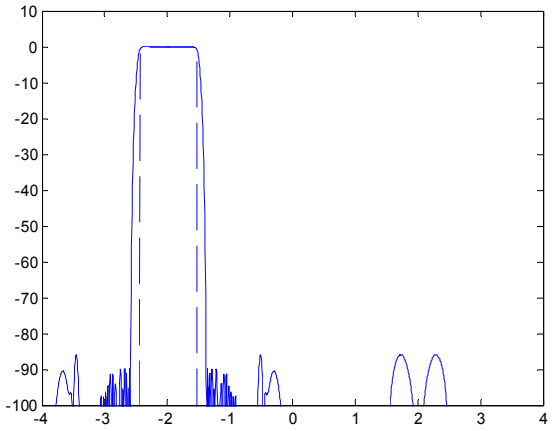


Figure 47. Interpolation/Modulation Combination of -2f_{DAC}/8 Filter in Odd Mode

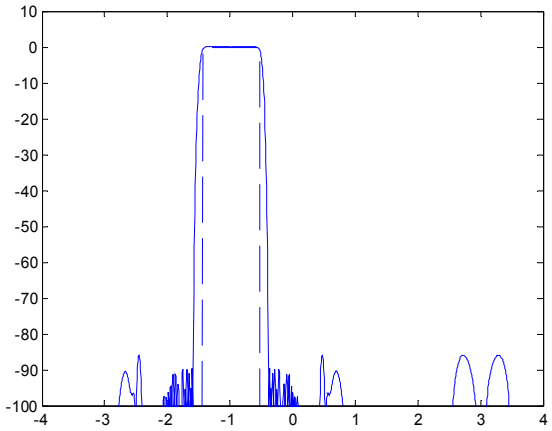


Figure 48. Interpolation/Modulation Combination of -1f_{DAC}/8 Filter in Odd Mode

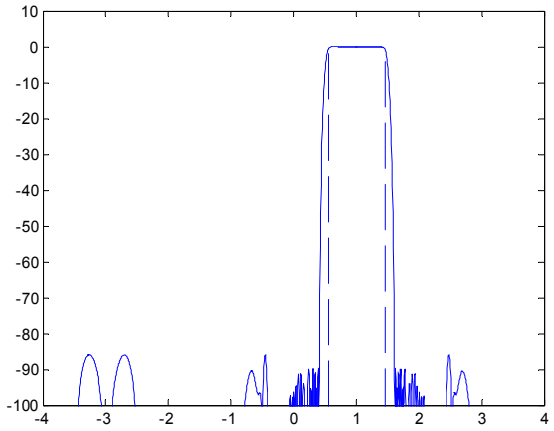


Figure 49. Interpolation/Modulation Combination of $f_{DAC}/8$ Filter in Odd Mode

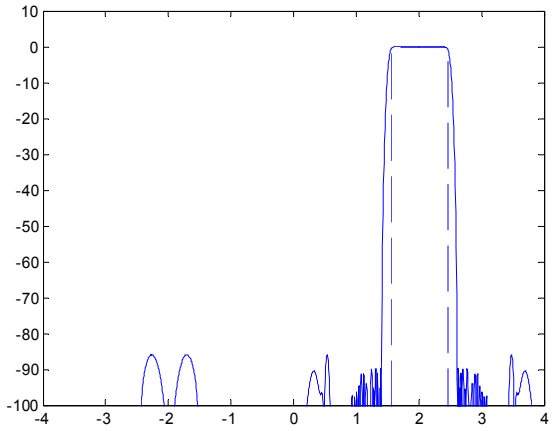


Figure 50. Interpolation/Modulation Combination of $2f_{DAC}/8$ Filter in Odd Mode

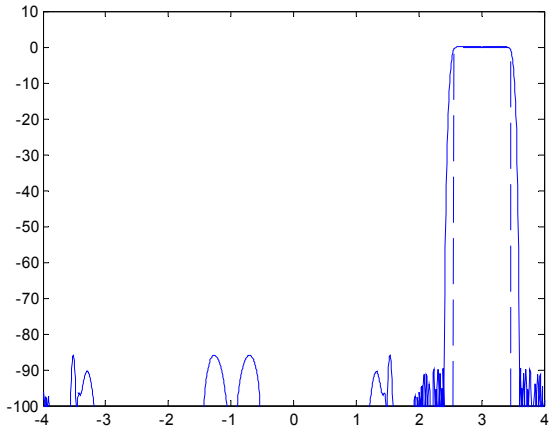


Figure 51. Interpolation/Modulation Combination of $3f_{DAC}/8$ Filter in Odd Mode

Even mode filter responses allow the passband to be centered around ±0.5, ±1.5, ±2.5 and ±3.5 F_{DATA}. Switching from and odd mode response to an even mode filter response does not modulate the signal. Instead, the pass band is simply shifted. As an example, picture the response of Figure 51, and assume the signal in band is a complex signal over the bandwidth 3.2 to 3.3×F_{DATA}. If the even mode filter response is then selected, the pass band will now be centered at 3.5×F_{DATA}. However, the signal will still remain at the same place in the spectrum. The even/odd mode capability allows the filter passband to be placed anywhere in the DAC Nyquist bandwidth.

The AD9779 is a dual DAC with an internal complex modulator built into the interpolating filter response. In dual channel mode, the AD9779 expects the real and the imaginary components of a complex signal at digital input ports one and two (I and Q respectively). The DAC outputs will then represent the real and imaginary components of the input signal, modulated by the complex carrier $F_{DAC}/2$, $F_{DAC}/4$ or $F_{DAC}/8$.

With reg 2, bit 6 set, the AD9779 accepts interleaved data on port one in the sequence I, Q, I, Q……. Note that in interleaved mode, that the channel data rate at the beginning of the I and the Q data paths are now ½ the input data rate, due to the interleaving. The max input data rate is still subject to the maximum specification of the AD9779. This limits the synthesis bandwidth available at the input to the AD9779 in interleaved mode.

With reg 02h, bit 5 (REAL MODE) set, the Q channel and the internal I and Q digital modulation are turned off. The output spectrum at the IDAC then represents the signal at digital input port one, interpolated by 1×, 2×, 4×, or 8×.

The general recommendation is that if the desired signal is within ±0.4*FDATA, that the odd filter mode should be used. Outside of this, the even filter mode should be used. In any situation, the total bandwidth of the signal should be less than 0.8*FDATA.

Using Data Delay to Meet Timing Requirements

In order to meet strict timing requirements at input data rates of up to 300MSPS, the AD9779 has a fine timing feature. Fine timing adjustments can be made by programming values into the DATA CLOCK DELAY register (reg 04h, 7:4). This register can be used to add delay between the DACCLK in and the DATACLK out. Figure 52 shows the default delay present when DATACLK DELAY is disabled. The disable function bit is found in reg 02h, bit 4. Figure 53 shows the delay present when DATACLK DELAY is enabled and set to 0000. Figure 54 indicates the delay when DATACLK DELAY is enabled and set to 1111. Note that the set up and hold times specified for data to DATACLK in the datasheet are defined for DATACLK DELAY disabled.

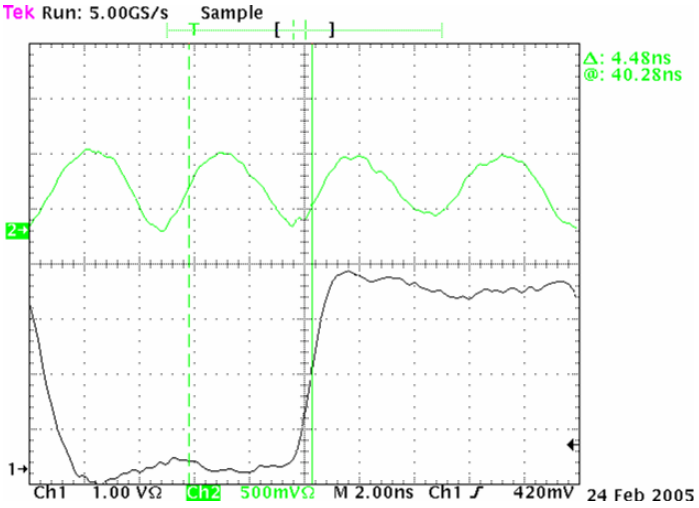


Figure 52. Delay from DACCLK to DATACLK with DATACLK DELAY disabled.

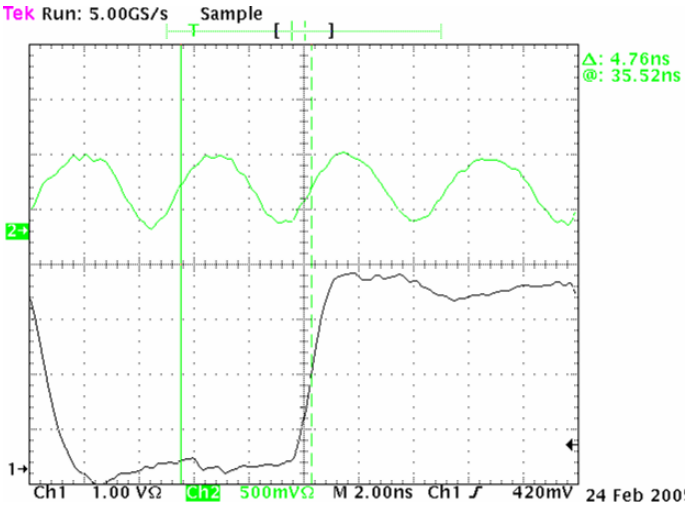


Figure 53. Delay from DACCLK to DATACLK out with CLK DATA DELAY = 0000

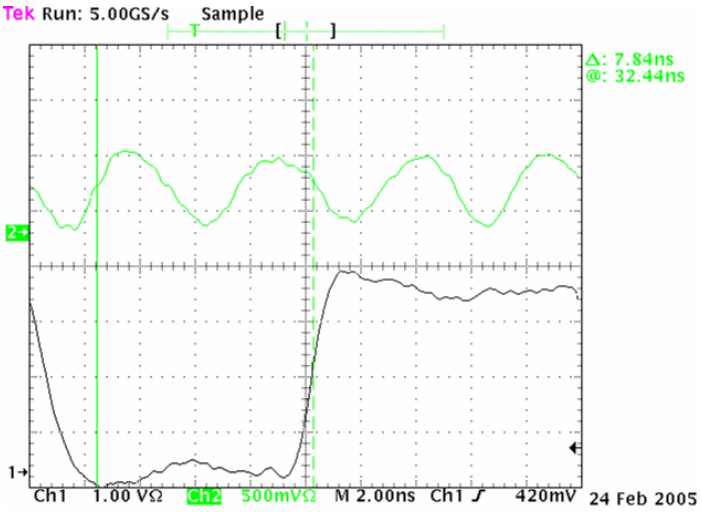


Figure 54. . Delay from DACCLK to DATACLK out with CLK DATA DELAY = 1111

The difference between the min delay of Figure 53 and the maximum delay shown in Figure 54 is the range programmable via the DATACLK DELAY register. The delay (in absolute time) when programming DATA CLK DELAY between 0000 and 1111 is a linear extrapolation between these two figures. (typically 175ps-225ps per increment to DATA CLK DELAY).

The frequency of DATACLK out depends on several programmable settings. Interpolation, zero stuffing and interleaved/dual port mode all have an effect on the DACCLK frequency. The divisor function between DACCLK and DATACLK is equal to;

Interpolation	Zero Stuffing	Input Mode	Divisor
1	disabled	dual port	1
2	disabled	dual port	2
4	disabled	dual port	4
8	disabled	dual port	8
1	disabled	interleaved	Invalid
2	disabled	interleaved	1
4	disabled	interleaved	2
8	disabled	interleaved	4
1	enabled	dual port	2
2	enabled	dual port	4
4	enabled	dual port	8

8	enabled	dual port	16
1	enabled	interleaved	1
2	enabled	interleaved	2
4	enabled	interleaved	4
8	enabled	interleaved	8

In addition to this divisor function, DATACLK can be divided by up to an additional factor of 4, according to the state of the DATA CLK DIVIDE register (reg 03h, 5:4), as follows;

Reg 03h (5:4)	Divider Ratio
00	1
01	2
10	4
11	1

The maximum divisor resulting from the combination of the above table, and the DATACLK divide register, is 32.

Data Input Synchronization

The AD9779 also allows the user to determine how close the data input timing is to the edge of the timing window (i.e., valid data set up and hold times). Figure 55 represents a functional block diagram of this circuitry. Data is effectively sampled at a time t_D before and after the clock edge. These two samples are compared. If both values are equal, the XOR gate will indicate a logic 0 for valid timing. Note that the Input Data Sampling Clock is the same signal as the DATACLK out, but without the delay programmed via the DATA CLOCK DELAY register. The time delay is programmable via register reg 03h, bits 3:0 (INPUT DATA TIMING ERROR TOLERANCE). The value of the XOR output is registered in reg 19h, bit 7 (DATA DELAY IRQ) when DATA DELAY IRQ ENABLE (reg 19h, bit 3) is true.

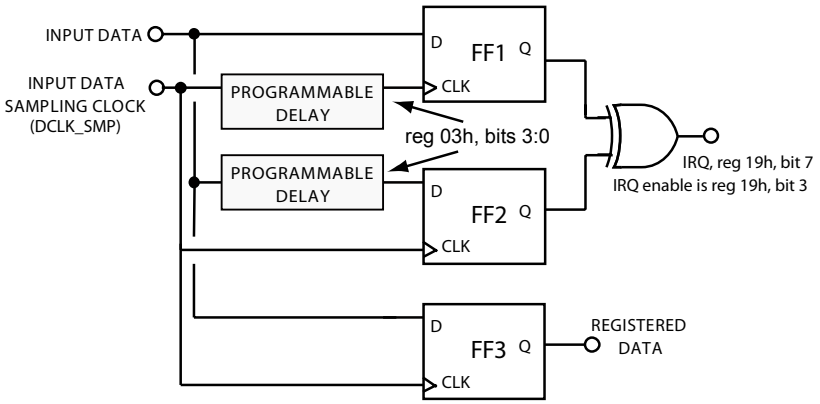


Figure 55 AD9779 Data Input Synchronization Logic

Manual or Automatic Input Timing Correction

Correction of input timing can be achieved manually, or the AD9779 can be programmed to automatically correct if it senses an error. The correction function is controlled via register 03h, bits 7:6. The function is programmed as follows;

Reg 03h (7:6)	Function
00	Error check disabled
01	Manual correction
10	Automatic, one pass check
11	Auto, continuous pass check

With manual correction, DATA DELAY IRQ must be polled to determine if timing is being violated. Necessary corrections can be made by adjusting DATACLK DELAY and the DATACLK INVERT bit (reg 2, bit 2). When doing initial timing verification, the user should set INPUT DATA TIMING ERROR TOLERANCE (reg 03h, 3:0) to 1111. DATACLK DELAY can then be swept to find the range over which the timing is valid. The final value for DATA DELAY should be the value that corresponds to the middle of the valid timing range. If a valid timing range is not found during this sweep, the user should invert the DATACLK INVERT bit and repeat the process. If a valid timing window is still not found, then INPUT DATA TIMING ERROR TOLERANCE should be decremented by one, and the procedure should be repeated.

In auto correction mode, the AD9779 will automatically sweep DATACLK DELAY as soon as the value 11 is programmed into

DATACLK DELAY MODE (03h, 7:6). The user should initially set INPUT DATA TIMING ERROR TOLERANCE to 1111, then set DATACLK DELAY to 11 to initiate the automatic timing sweep. The AD9779 will then sweep DATACLK DELAY from 0000 to 1111. If the value for IRQ initially indicates that the timing is valid (set up and hold times are being met) then the sweep will stop immediately. Otherwise, the sweep will continue until IRQ indicates that the timing is valid. If the sweep completes and a valid timing region is not found, then the user should invert DATACLK INVERT and repeat the operation. If this is still not successful, then the user should decrement INPUT DATA TIMING ERROR TOLERANCE and rewrite 11 to DATACLK DELAY MODE.

Multi-DAC Synchronization

SYNC Pulse Generation (Master Devices)

In applications where multiple AD9779s are used, and need to be synchronized together, the AD9779 provides a flexible synchronization engine. There are two options for multi DAC synchronization. In the first situation, one AD9779 can be used as a master, and the rest of the AD9779 devices as slaves. The second option is that all the AD9779 devices operate as slaves. Both operations have the same timing restrictions, and there are no performance tradeoffs for either mode. The following text describes the Master mode. The differential input clock will drive the master device, and the master will in turn generate SYNC_O+ and SYNC_O-. These two signals use LVDS levels to generate a differential synchronization signal, which will in turn be used to synchronize all of the slave AD9779 devices. SYNC_O+ and SYNC_O- must loop back to the sync inputs (SYNC_I+ and SYNC_I-) of the master for multiple device synchronization. The master mode is enabled by writing the Sync Driver Enable bit (reg 07h, bit 6) to a logic 1. The SYNC_O signal speed can be an integer divisor of the DACCLK speed, according to reg 04h, 3:1. Enabling the AD9779 in slave mode is accomplished by writing the Sync Receiver Enable bit (reg 07 bit 7) to a logic 1. The timing of the DAC input clock and the SYNC output signals on the master device are shown in Figure 56.

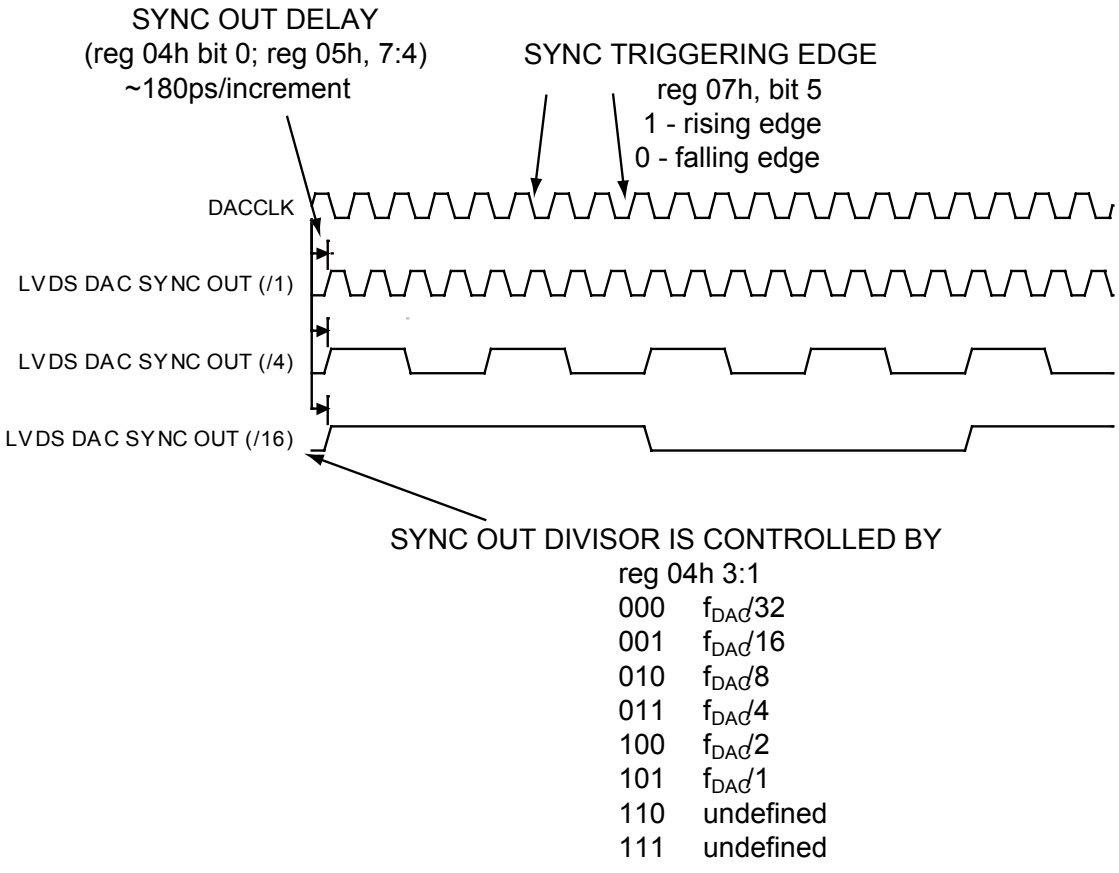


Figure 56. AD9779 DACCLK/SYNC Output Timing

The SYNC output pulse must then be distributed from the master to all of the slave devices. This may require that the user implement circuitry outside of the AD9779 that splits the LVDS signal. The splitter delivers the SYNC_O signal from the master to the multiple slave device SYNC_I pins. A block diagram of this implementation is shown in Figure 57. The equalization from the CLK source and SYNC_O to the DACCLK and SYNC inputs of the multiple AD9779 devices is critical. For the multi-chip synchronization to operate correctly at maximum specified DAC sample rates, the DACCLK inputs must be phase aligned to ±100ps. The SYNC_I inputs must also be phase aligned to ±100ps. At lower DAC sample rates, this timing alignment can be relaxed

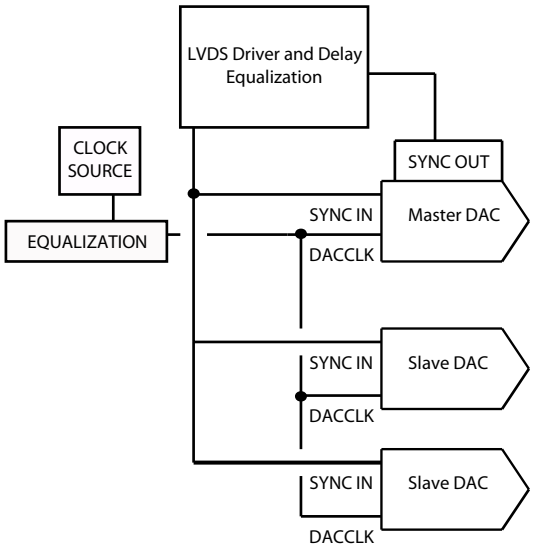


Figure 57. Implementation of SYNC Signal Distribution in Master/Slave mode

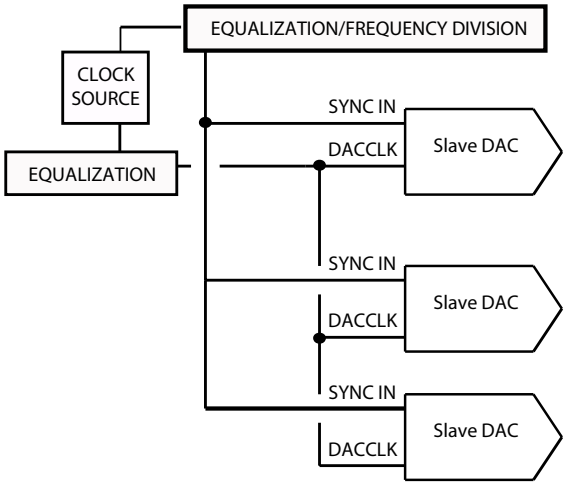


Figure 58. Implementation of SYNC Signal Distribution in Slave mode

SYNC Pulse Receiver (Slave Devices)

The following description of SYNC_IN on the AD9779 slave devices also applies to the SYNC_I on the master device. The timing for SYNC_I on the master must match that of the slave devices. The SYNC IN pulses, as shown in Figure 57, are not restricted as to their duty cycle. The only restriction is that each SYNC pulse remain high for at least one DACCLK cycle. However, the slave DAC receiving the SYNC pulse must know what the speed of the input SYNC pulse is. The ratio of DACCLK to SYNC_I speed is determined by the values in INPUT SYNC PULSE FREQUENCY (reg 05h, 3:1) as follows;

Reg 05h, 3:1	Divider ratio
000	DACCLK/32 (default)
001	/16
010	/8
011	/4
100	/2
101	undefined
110	undefined
111	undefined

Internal Synchronization in Slave Device

The internal timing functions in the slave AD9779 are given in Figure 59. The duty cycle of the SYNC_I signal is not restricted to 50%. The minimum restriction on duty cycle for SYNC_I is that it stays high for at least one full DACCLK cycle. Figure 59 shows two possible SYNC_I signals, one with 50% duty cycle, and one with minimum duty cycle. More detail on SYNC_I timing restriction are given later in this section.

DACCLK samples SYNC_I and generates the internal SYNC signal (SYNC_I_int). The period of SYNC_I_int is always DACCLK/32. If the rate of SYNC_I is greater than DACCLK/32, then the extra pulses are stripped off. The example Figure 59 shows SYNC_I period = DACCLK/16, so that every other SYNC_I pulse is stripped. DCLK_SMP is the input data sample clock, originally defined in Figure 55. DCLK_SMP is synthesized by DACCLK, but synchronized by SYNC_I. Note that there is also a programmable delay (SYNC INPUT DELAY) between SYNC_I_int and DCLK_SMP. This programmable delay adds even more flexibility to the timing interface. The example in Figure 59 indicates that the interpolation is set to 8× (DCLK_SMP rate is 1/8 that of DACCLK).

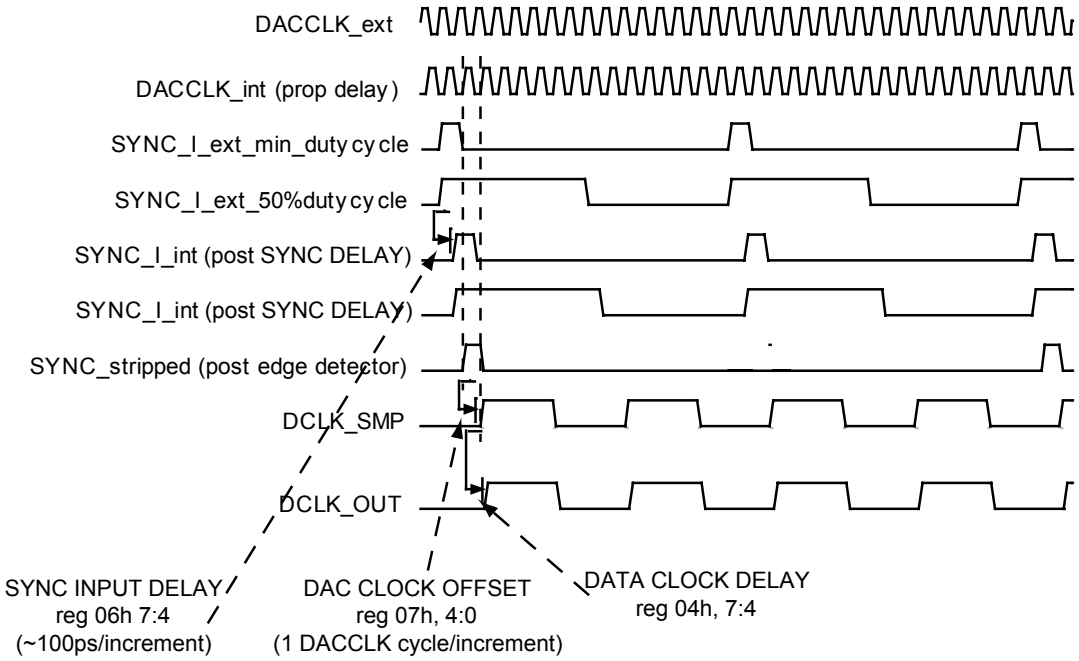


Figure 59. Internal and External Timing for AD9779 Master or Slave

SYNC_I Timing Restrictions

In the same way that the AD9779 registers timing errors for the data input, it can also register timing errors for the SYNC_I signals. The block diagram for this synchronization logic is given in . This is very similar to the data input synchronization circuit given in Figure 59. The difference is that this circuit uses the DACCLK to properly register SYNC_I. The delay is programmable via reg 06h, 3:0. IRQ is registered in reg 19h, bit 6.

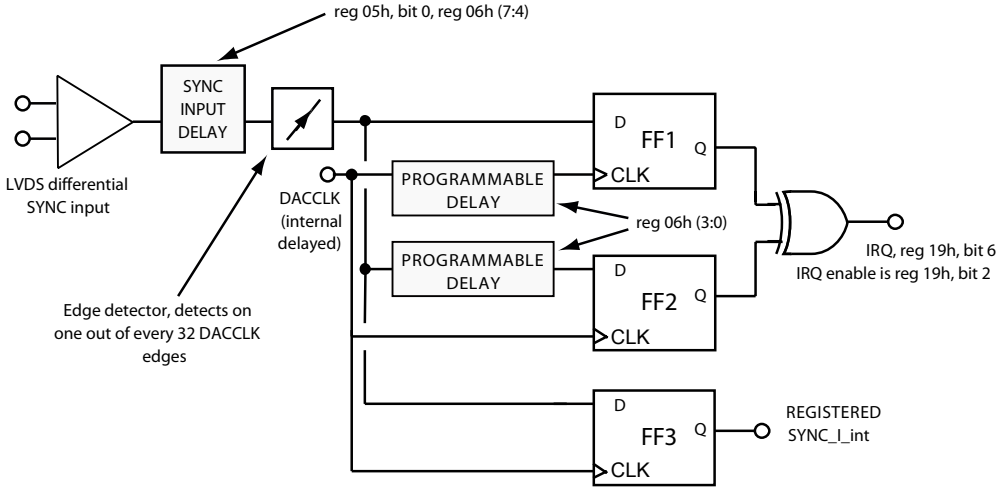


Figure 60. AD9779 Simplified Internal Synchronization Logic

EVALUATION BOARD SCHEMATICS

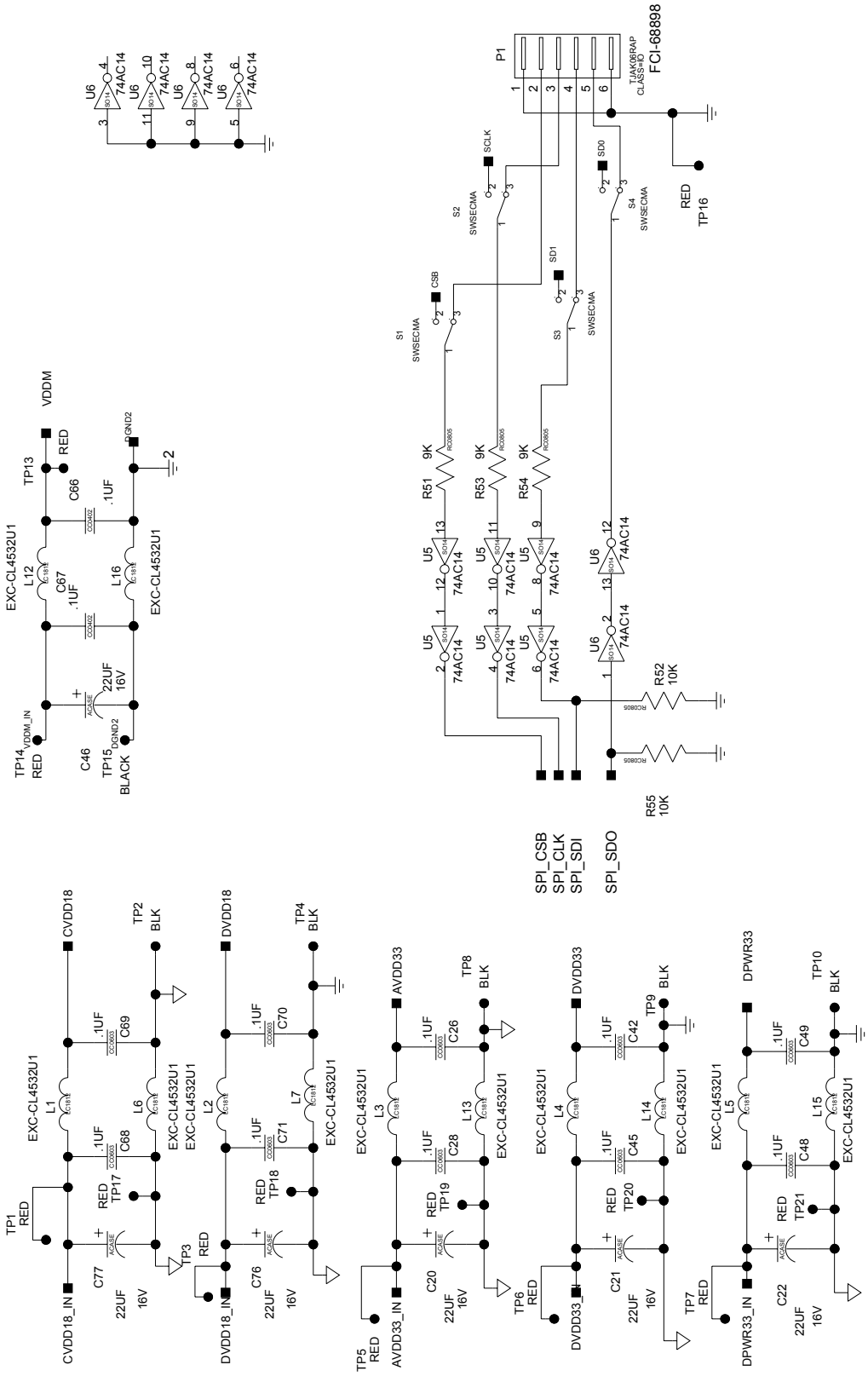


Figure 61. AD9779 Eval Board, Rev D , Power Supply Decoupling and SPI Interface

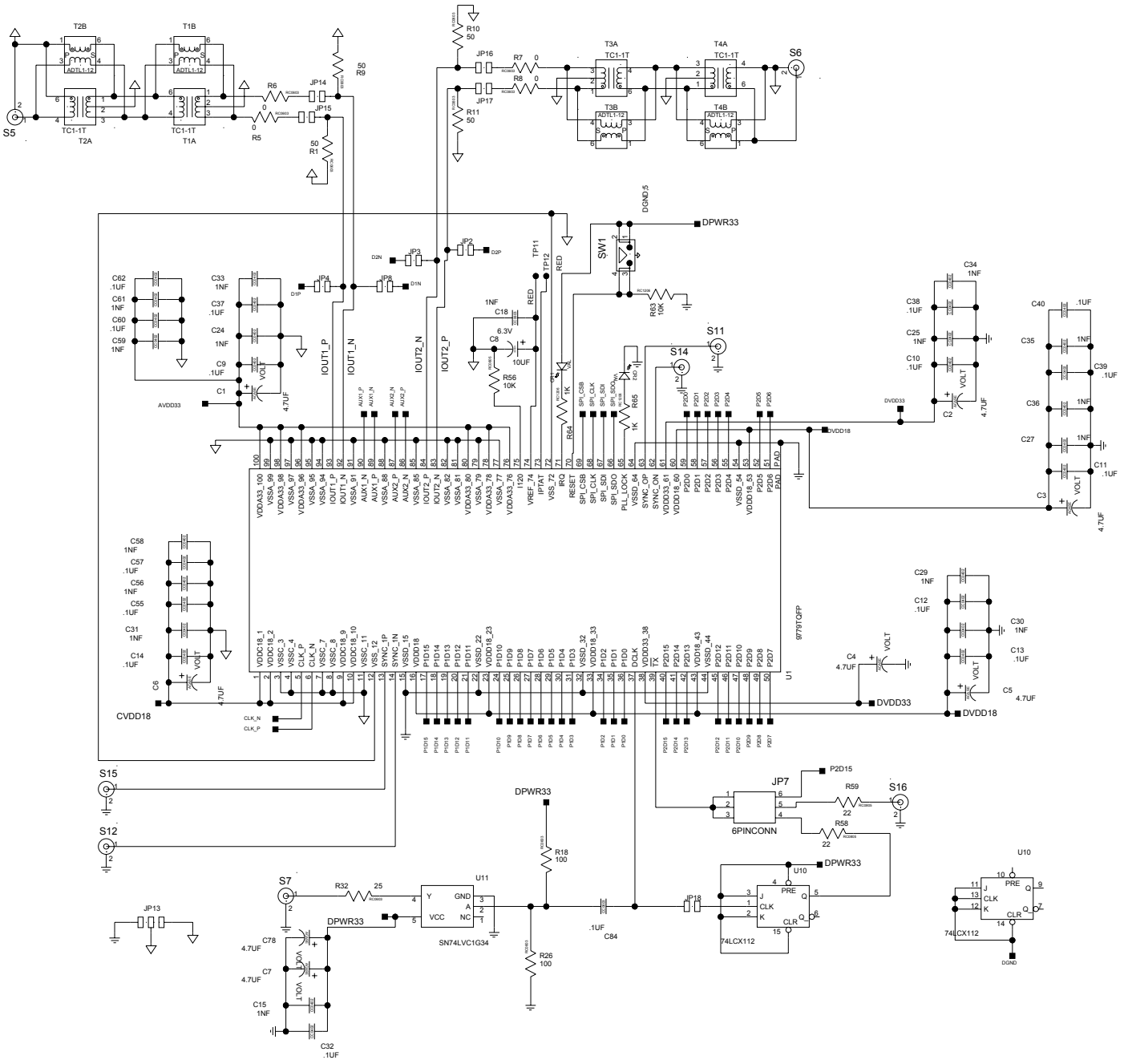


Figure 62. AD9779 Eval Board, Rev D , Circuitry Local to AD9779

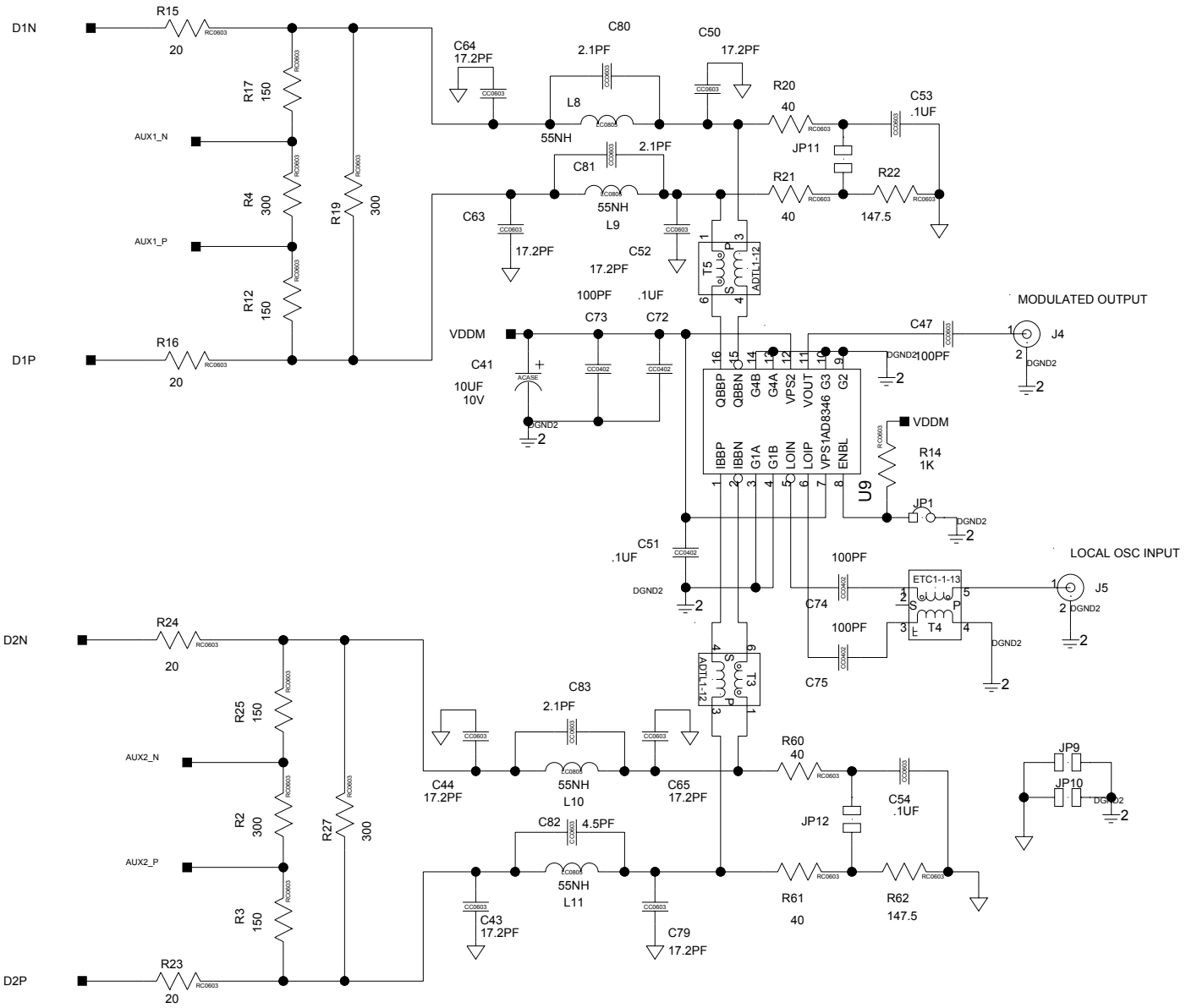


Figure 63. AD9779 Eval Board, Rev D , AD8349 Quadrature Modulator

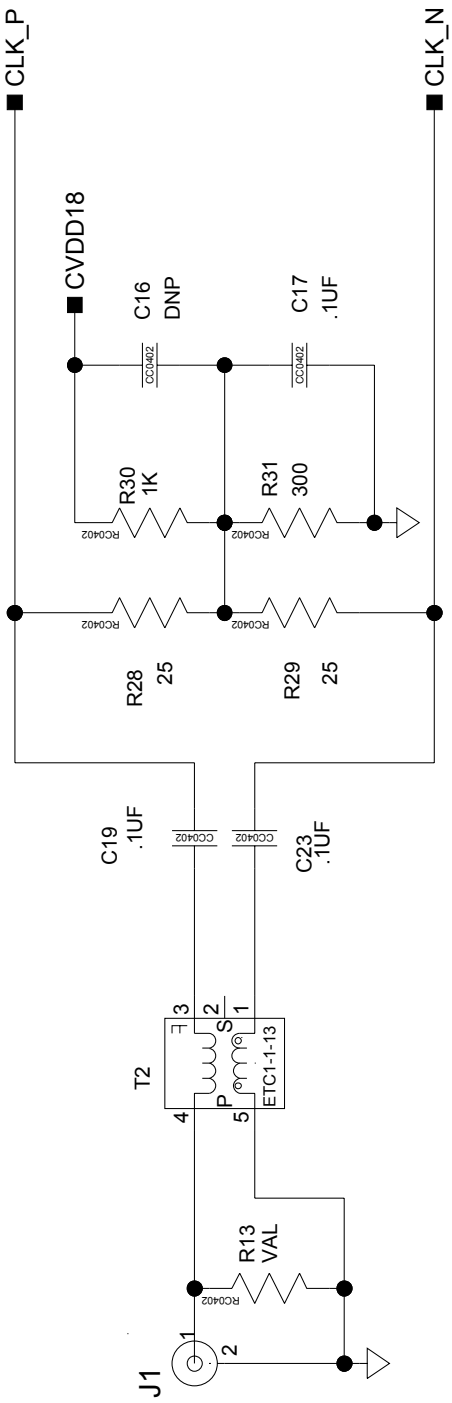


Figure 64. AD9779 Eval Board, Rev D , DAC Clock Interface

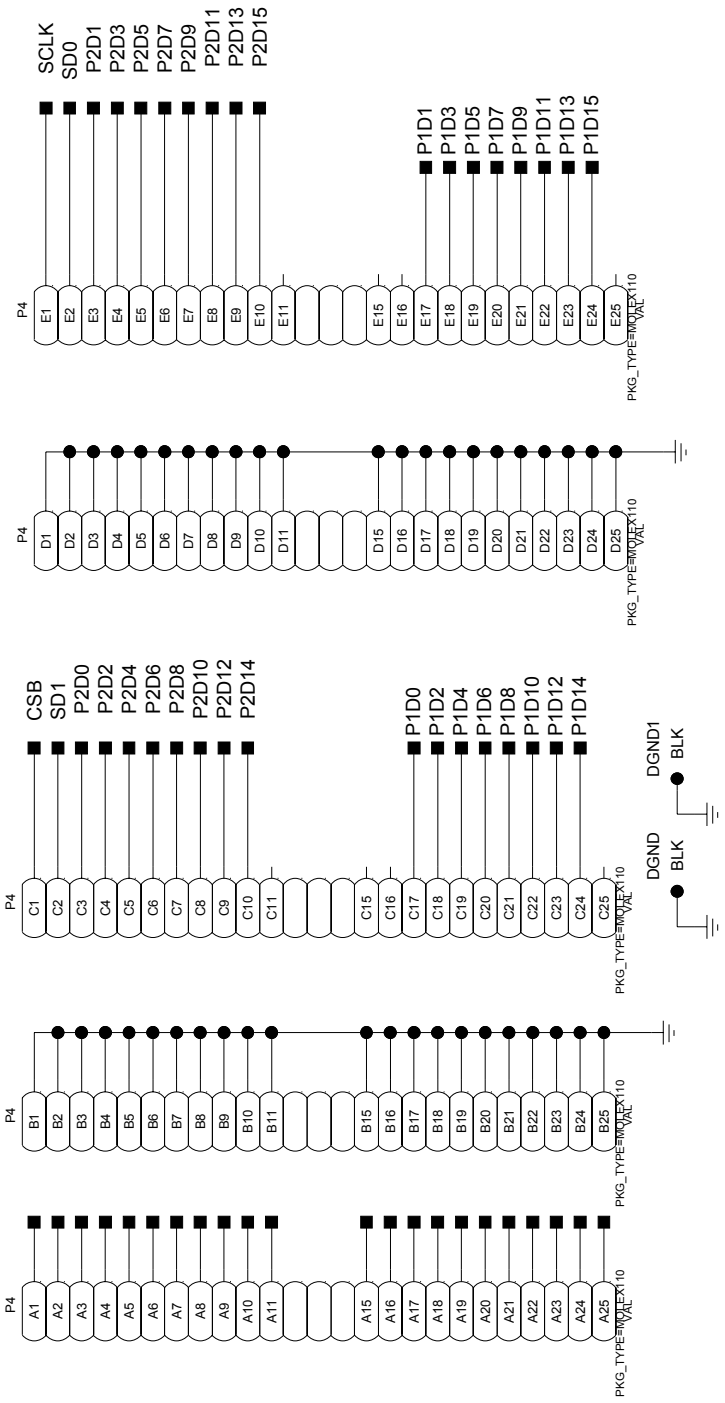


Figure 65. AD9779 Eval Board, Rev D, Digital Input Buffers

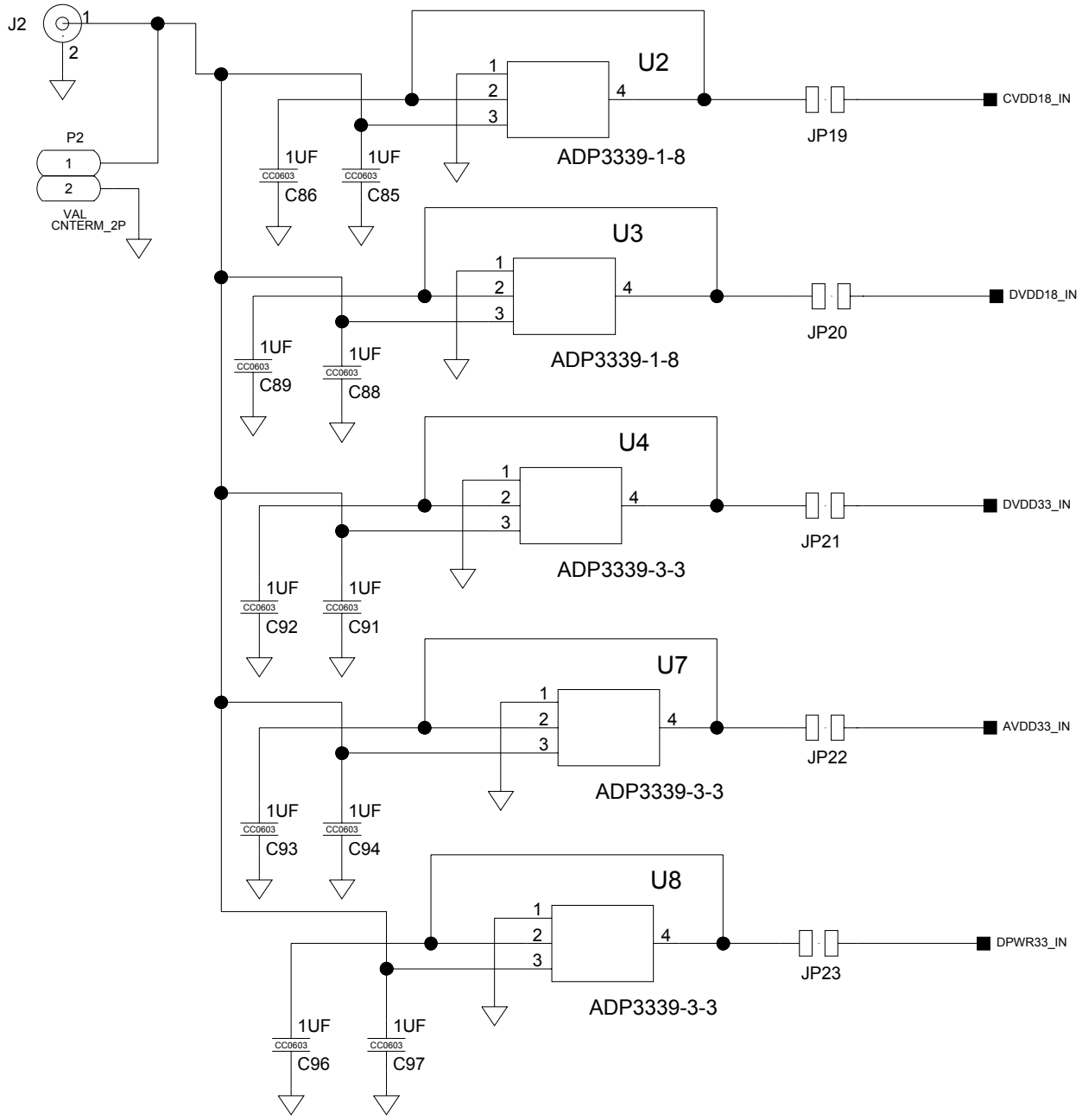


Figure 66. AD9779 Evaluation Board, on board voltage regulators

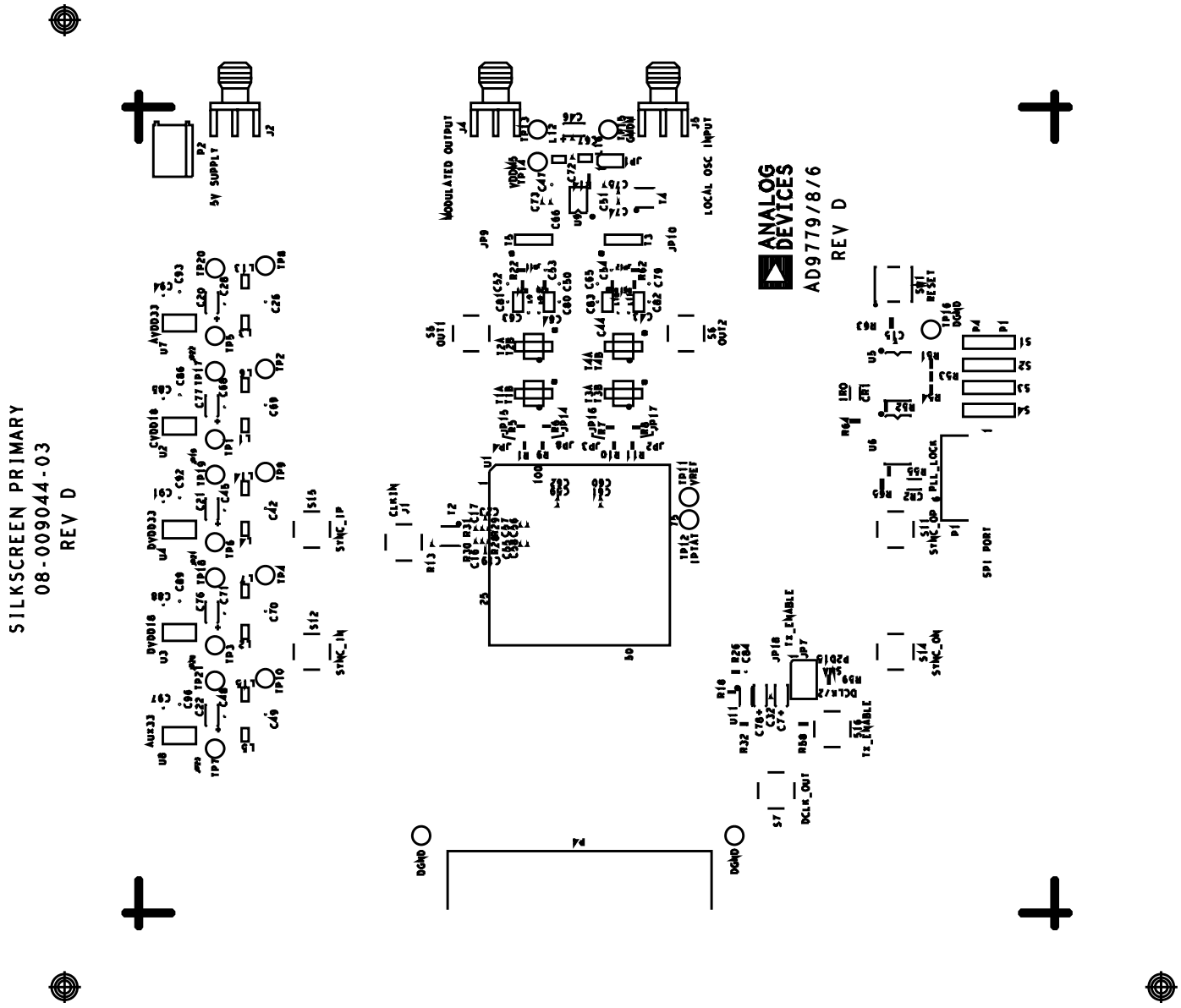


Figure 67 AD9779 Rev D Eval Board, Top Silk Screen

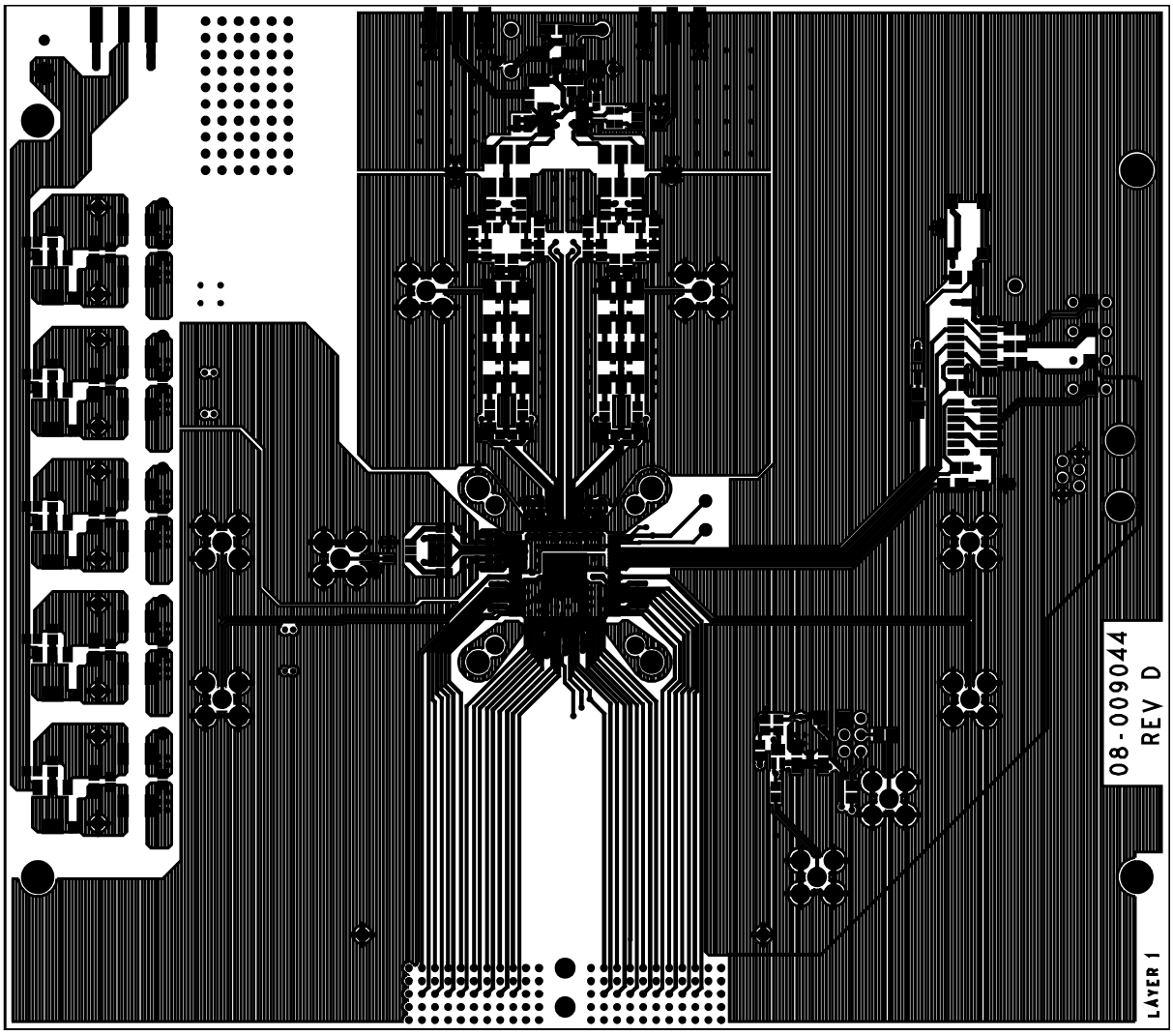


Figure 68. AD9779 Rev D Eval Board, Top Layer

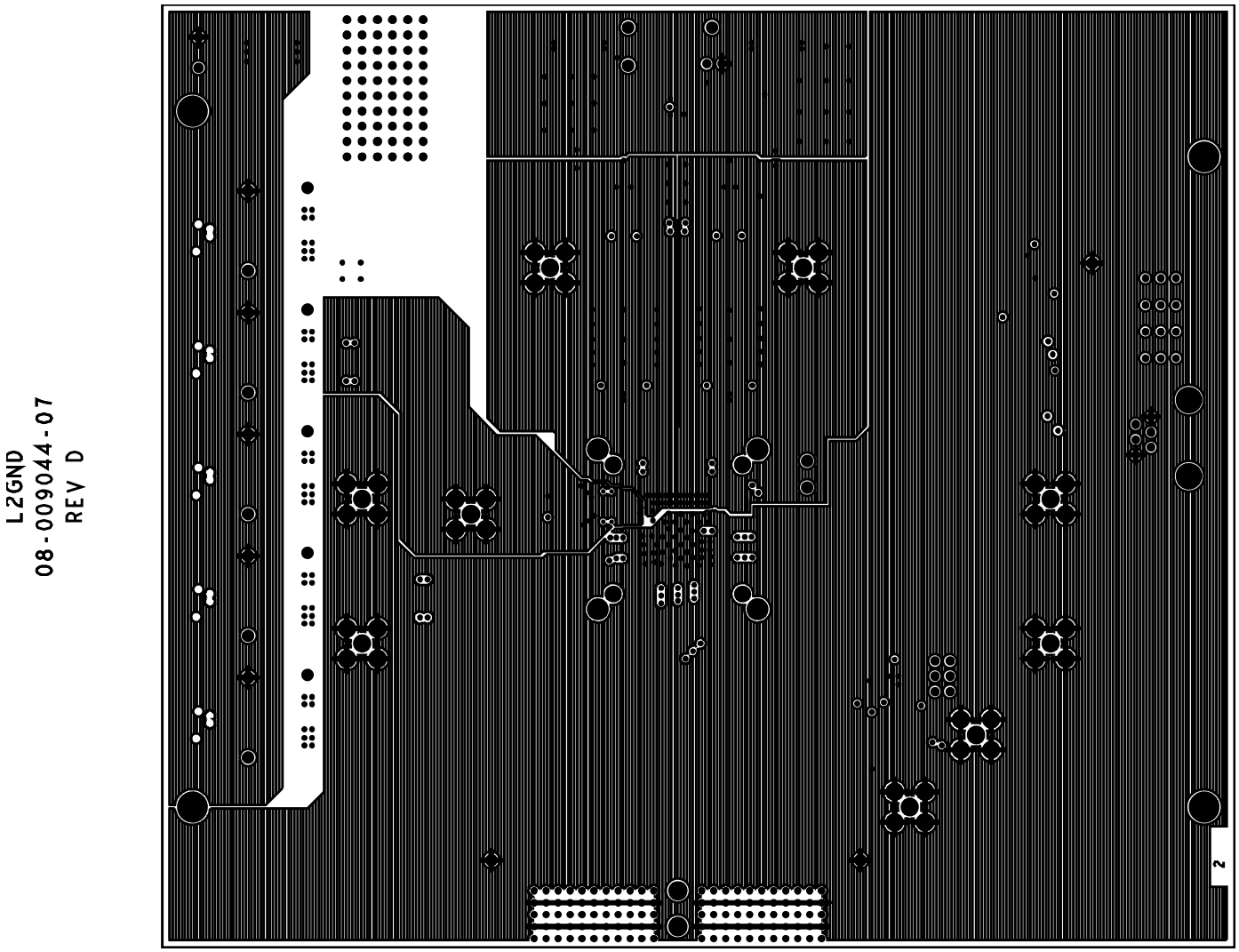


Figure 69. AD9779 Rev D Eval Board, Layer 2

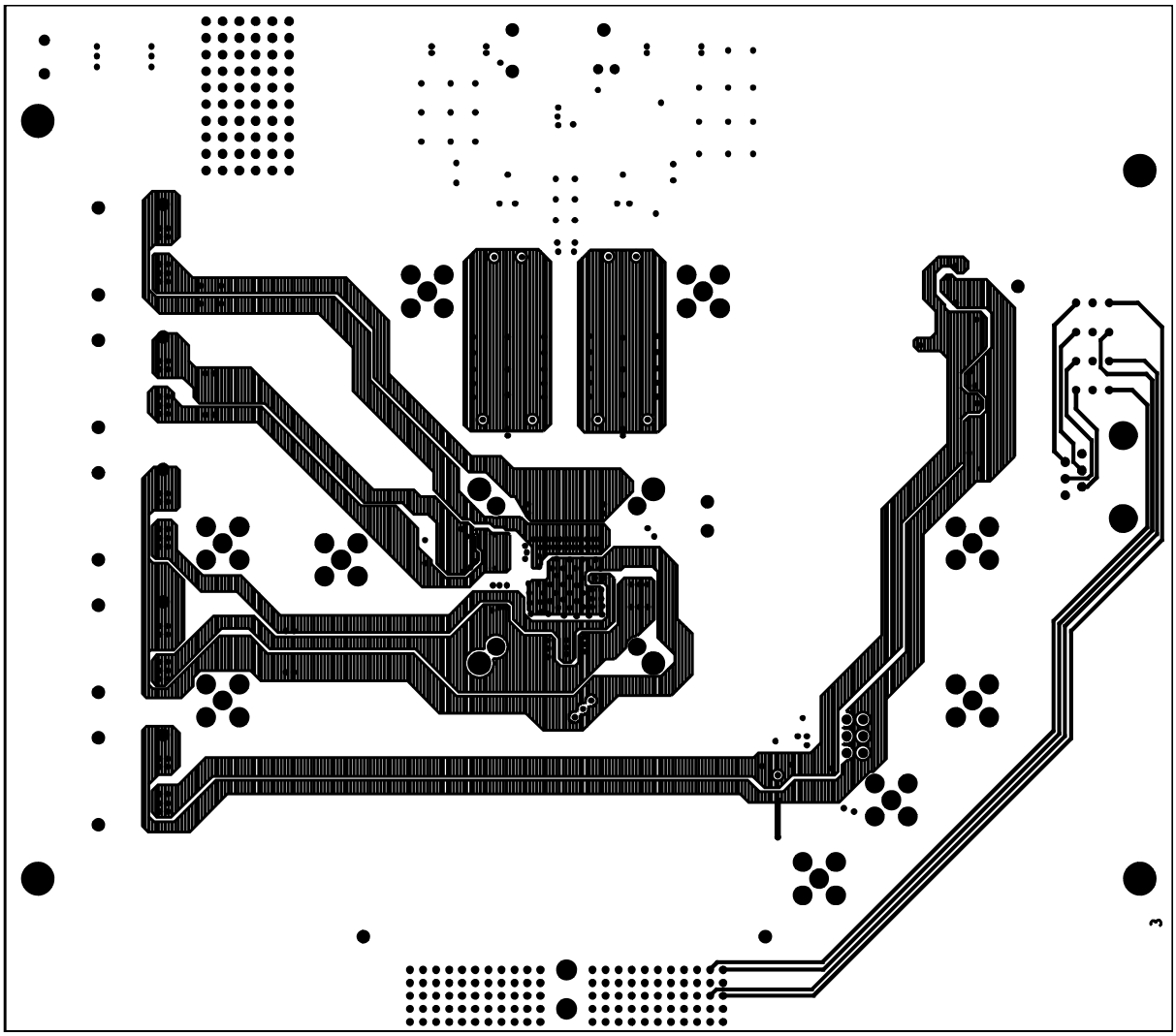


Figure 70. AD9779 Rev D Eval Board, Layer 3

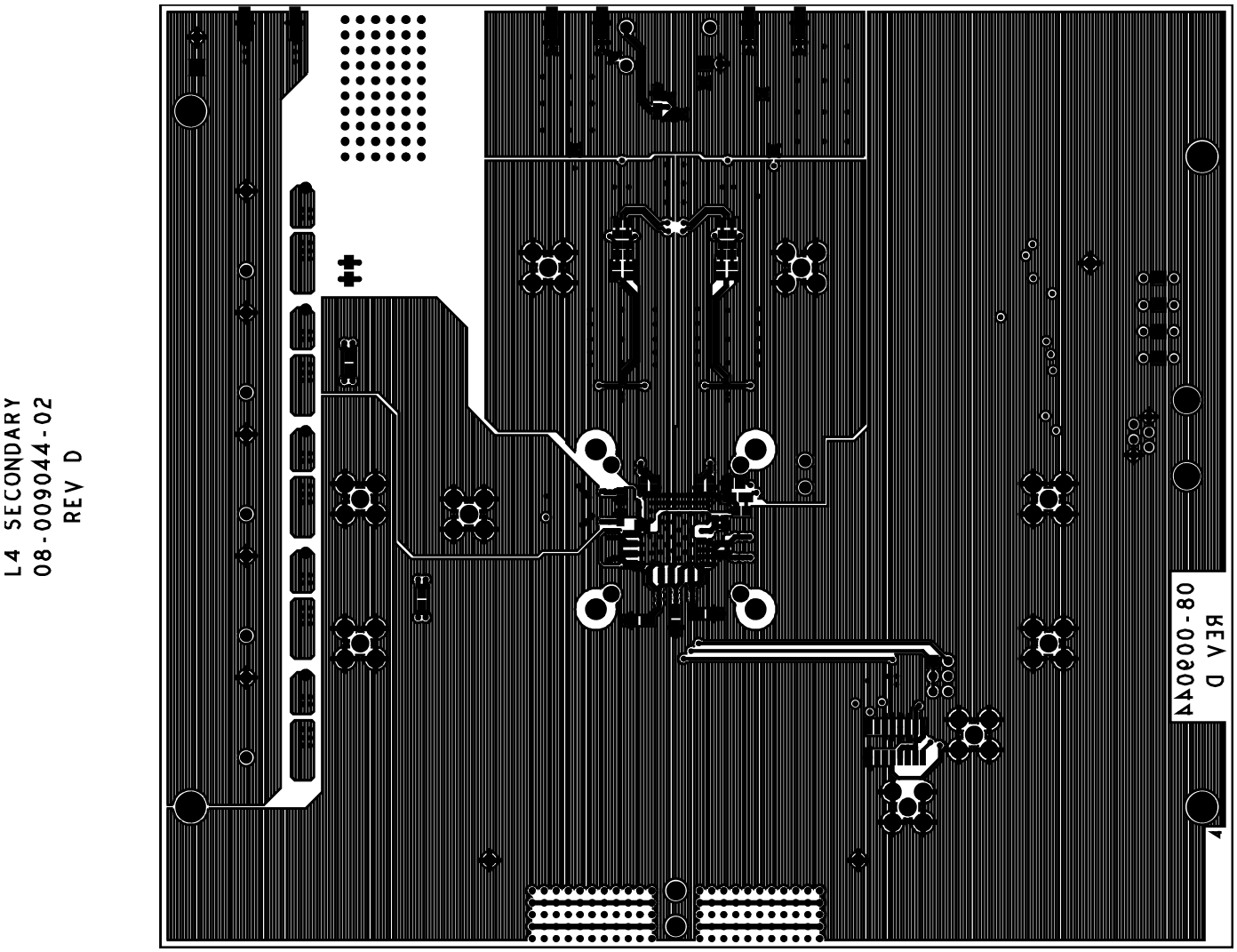


Figure 71. AD9779 Rev D Eval Board, Bottom Layer

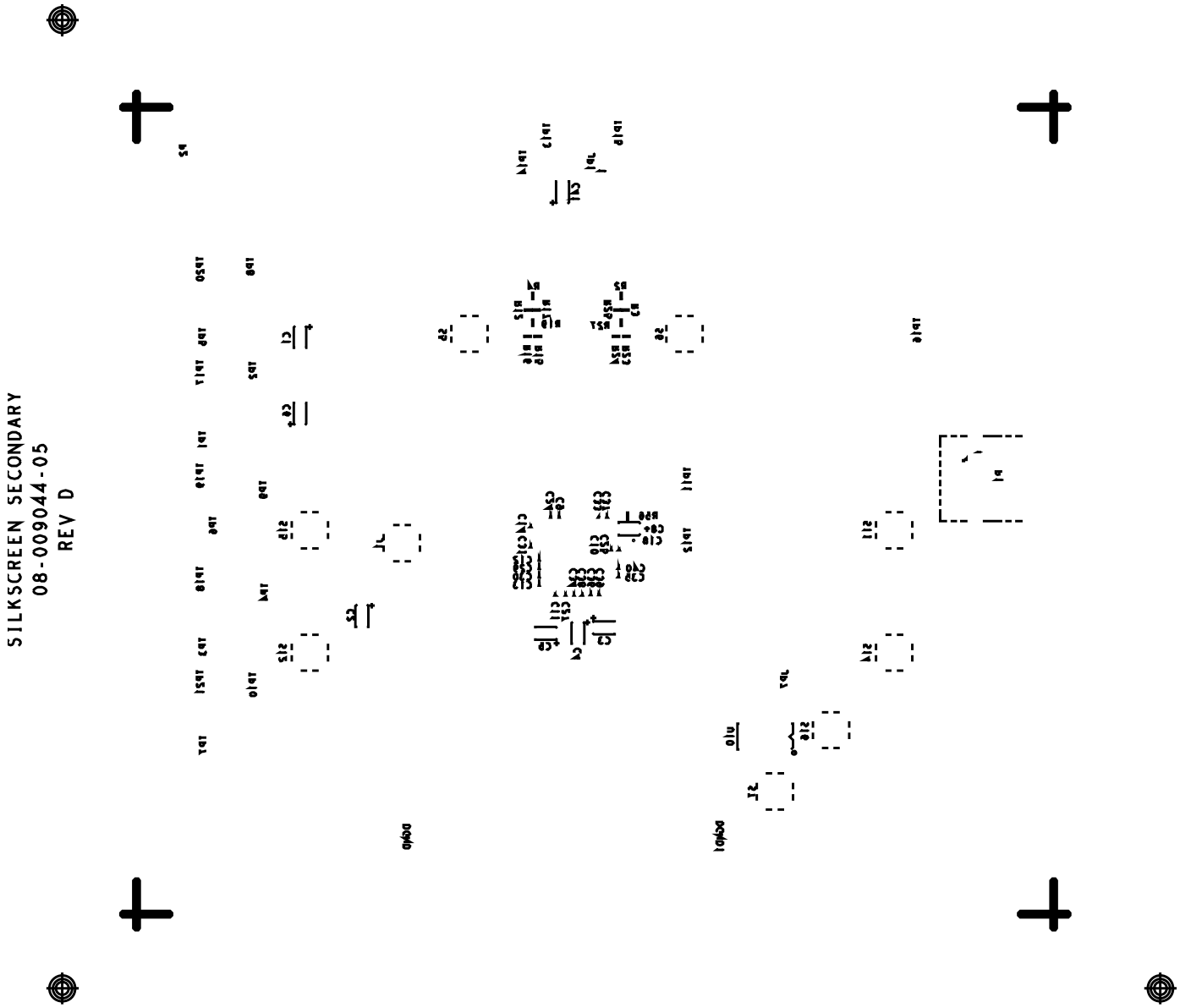
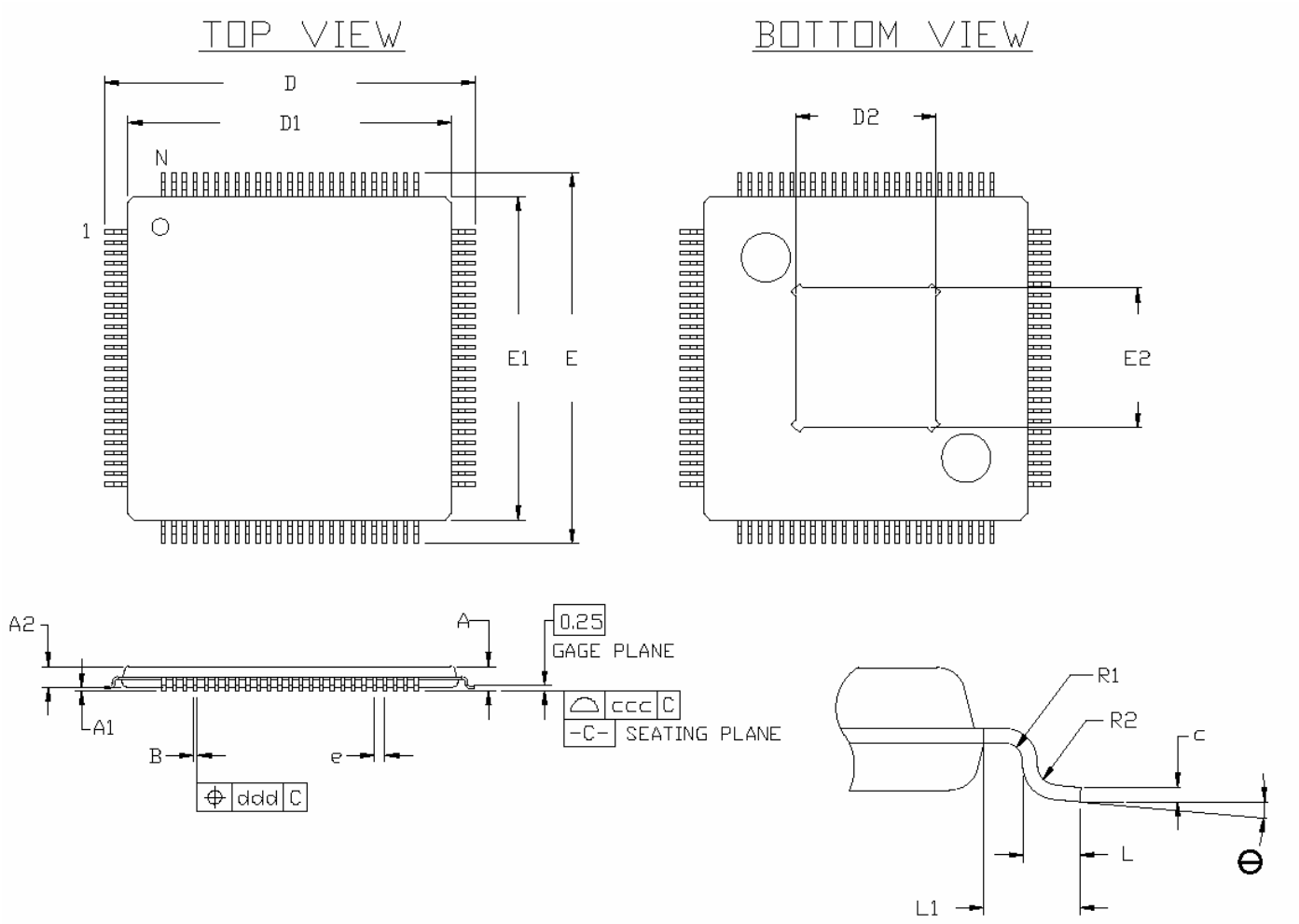


Figure 72. AD9779 Rev D Eval Board, Bottom Silkscreen

Outline Dimensions



NOTES:

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1. Controlling Dimensions are in mm.
2. All dimensions per JEDEC Standards MS-026-Variation.
3. Inverted Form is Paddle Up and Die Down

COMMON DIMENSIONS			
Dim	**Min.**	**Nom.**	**Max**
A			1.20
A1	0.05		0.15
A2	0.95	1.00	1.05
L	0.45	0.60	0.75
L1		1.00 REF	
Θ	0^0	3.5^0	7^0
R1	0.08		
R2	0.08		0.20
c	0.09		0.20

14X14X1.0(OPTION 2)				
N = 100 Leads				
Variation AED(see note 2)				
Dim	Min	Nom	Max	Note
e		0.50 BSC		
D2		9.5		
E2		9.5		
D	15.80	16.00	16.20	
D1	13.80	14.00	14.20	
E	15.80	16.00	16.20	
E1	13.80	14.00	14.20	
B	0.17	0.22	0.27	
ccc		0.08		
ddd		0.08		

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Warning---Please not that this device in its current form does not meet Analog Devices' standard requirements for ESD as measured against the charged device model (CDM). As such, special care should be used when handling this product, especially in a manufacturing environment. Analog Devices will provide a more ESD-hardy product in the near future at which time this warning will be removed from this datasheet.

PR05363-0-4/05(PrG)

ORDERING GUIDE

Model	Temperature Range	Description
AD9779BSV	-40°C to +85°C (Ambient)	100-Lead TQFP, Exposed Paddle
AD9779BSVZ		100-Lead TQFP, Exposed Paddle, Lead Free
AD9779BSVZRL		100-Lead TQFP, Exposed Paddle, Lead Free, reel
AD9779-EB	25°C (Ambient)	Evaluation Board

Table 15: Ordering Guide